TIMING SYSTEMS SESSION SUMMARY

Chair: Yang Fumin

More Event Timers are available, for 2 KHz and even higher repetition rates:

- A032-ET from Latvia, precision 10 ps, 10 KHz
- P-PET-C from Prague, Czech Republic, precision 2.5 ps, 2 KHz
- T2L2 ET from OCA, France, precision 2 ps, ~2 KHz
- ET from HTSI, USA, precision 2 ps, ~50 KHz

With much improved linearity and thermal drift.

Question: Are the prices for these ETs available?

Y. Zhang from Shanghai showed in a poster that only one FPGA chip can work as a timer for future space applications or other compact systems.

A032-ET Experimental Test on Changchun SLR

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Abstract

This paper introduces the experimental test of A032 Event Timer on Changchun SLR. First, the pulse delay generator DG535 is used to generate two path signals to simulate the start and stop signal, and the A032-ET to measure the intervals. Then, it also gives out the system hardware connection diagram, analyzes signal time sequence and shows the software flow chart. Finally it shows the results of ranging the ground target and the satellites.

Key Words: Event Timer, A032-ET, Satellite Laser Ranging (SLR), Simulation

Introduction

Satellite Laser Ranging (SLR) is the most accurate satellite tracking technique available with single shot positional accuracy under a centimeter and normal point corrected data able to claim precision of just a few millimeters. The SLR tracking method requires a pulsed laser source and a telescope which is used to collect the reflected laser light on its return. The laser provides a detectable link between a fixed station and a distant satellite moving in the space. The telescope and associated equipment determine a very precise location and velocity for both the satellite and station from the data provided by the laser beam. Time interval from station to the satellite and back can be calculated by counters, which is transferred into the range we want.

The SLR data are used to improve the orbital predictions for the tracked satellites which, in turn, make the satellites easier to track. In other words, the more data we get the better precision of orbit prediction we can calculate. Increasing the firing frequency is a convenient way to increase data, and there are many stations around the world trying to do KHz SLR system. SLR, in essence, is a method of satellite tracking. The key equipment for increasing the firing frequency are the counter and laser source. But now the KHz laser source is available in the world. And here we put the emphasis on the counter. There are two kinds of counters: the Time Interval counter and the Event Timer counter. The interval counter measures the time the laser flight from the station to satellite and back. HP5370 and SR620 are the most popular used interval timers in the global SLR society. The Event Timer records the epochs of signals received by both channel A (start) and B (stop) and puts them into buffer. Then the epochs are matched by range gate prediction. Event Timer calculates intervals with epochs, and in theory, with no rate limits but reading and processing data.

While using Event Timer, sending range gate is the most important technical difficulty, and the match of start and stop signals is also very important. Many stations in the world are adopting Event Timer as counter to advance their systems. PET4 has been used in Wettzell station, which is assembled by Dassualt model; P-PET 2000 begun to work in San Fernando in 2004, and Graz station have already completed KHz system; the KHz system in Herstmonceux is on developing stage, and almost finished. A032-ET developed by Latvia University using EET method also fits for KHz system in theory.

Status In Changchun

There are two interval counters in Changchun station: HP5370B is used routinely and SR620 as a standby. The observation in Changchun is excellent these years and the system is steady. The single shot precision is less than 2cm, and the passes observed every year are more than 4,000. However, the laser fire frequency is not very high: 8Hz for low orbit satellites and 5 Hz or 4Hz for high orbit satellites. We plan to use the Event Timer to increase firing frequency to 10Hz and even higher so as to increase the quantity of data. After analyzing all Event Timers, the A032-ET was chosen for Changchun experiment, and the purpose is to increase the firing frequency for all satellites to 10Hz, and even higher. As an Event Timer, A032-ET is superior to interval counter; some specifications are shown in Table 1.

Table 1: *A032-ET specifications*

Single shot RMS		<10 ps
Dead time		60 ns
Nor-linearity error		< 1 ps
Offset temperature stability		<0.1 ps
FIFO depth		1,200
Measurement rate	Option 1	Up to 10KHz continually
	Option 2	Up to 500Hz cycle repetition rate

Figure 1. *Hardware of A032-ET*

There are two currently available options of the A032-ET, which use the same specialized hardware (Figure 1 shows the hardware of A032-ET) but differ by the software. These options provide alternatively two basic kinds of measurement: The option A032.1 provides continuous (gapless) measurement of events at high (up to 10 KHZ) mean measurement rate. It is well suitable to measure the overlapped time intervals between Start and Stop events that come at the separate inputs (either A or B) of the Event Timer in any order. Specifically this is the case of advanced SLR at KHz repetition rate. The option A032.2 provides cyclical measurement of events that come at the separate inputs of the ET-device in the strict order. Specifically this is the case of conventional SLR where the measured Start-Stop time intervals do not exceed the repetition period of Start events. Considering our purpose, we choose A032.1 option to do the experiment, and the range gate has to be redesigned to fit for the new counter.

Experiment test and real observation on Changchun SLR

Before experiment we redesign the range gate control circuit, and the scheme is represented in Figure 2.

Range gate control circuit is assembled by three circuits, which are designed by the same module. The three circuits generate gate signal circularly and then are imported into an OR gate. Finally, the RG_out is transmitted as the range gate we want.

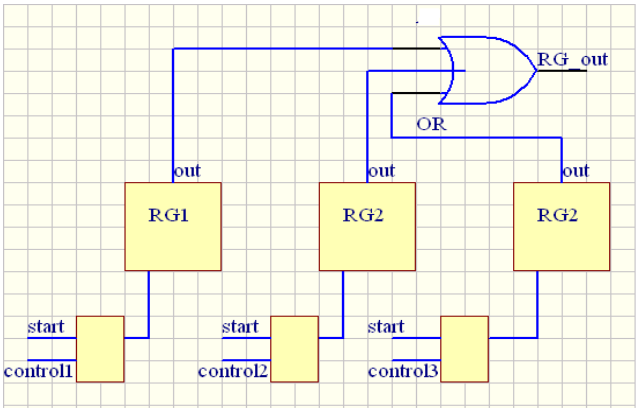
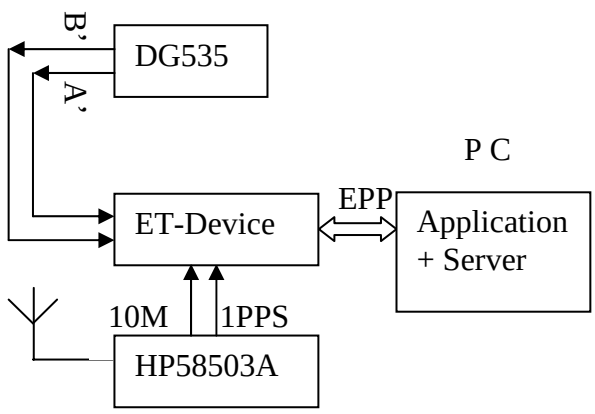


Figure 2. *Range gate control circuit*

Simulation

In this simulation, we use pulse generator DG535 as a signal source. It generates two NIM signals, and the interval was measured by A032-ET. The rate is set to 10Hz for the purpose is increasing the frequency to 10Hz. The interval sent by DG535 is static and the trigger is interior. The hardware connection scheme is shown in Figure 3, and the software flow chart is showed in Figure 4. All through the test, A032-ET worked normally, it measured the interval with the precision of ps under the condition of 10Hz



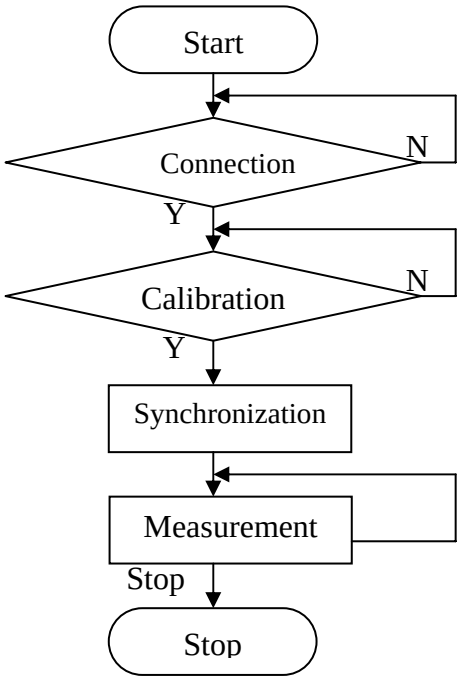


Figure 3. *Simulation scheme*

Figure 4. *Software flow chart*

Range gate measurement

Range gate is measured with A032-ET to find out the matching of start and stop signals. In this experiment, the start pulse is generated by DG535, which is triggered by laser firing, and output of the range gate is used as the stop pulse. Range gate measurement is to simulate observation condition and make some improvement for the software. The main function written in VC++ language is compiled as Dynamic Link Library. The data received by A032-ET is transferred into control software written in VB for

calculating the time interval. The data transferred into VB with the form of an array included time-tags that the events happened in channel A, B. The time-tags are matched well with range gate prediction.

Real Observations

The firing frequency is increased to 10Hz for all satellites and A032-ET is used as a new timer to calculate the time interval instead. The hardware connection scheme is presented in Figure 5. The main pulse is imported into channel A as start signal and the return pulse as stop signal. A032-ET could distinguish only NIM pulses; the 10MHz and 1pps signals are given by GPS HP58503A. Figure 6 shows the time sequence of Changchun SLR system. In the scheme, T1 and T4 is laser fire time, T2 is the epoch time of the main pulse, and T3 is the epoch time of the return pulse.

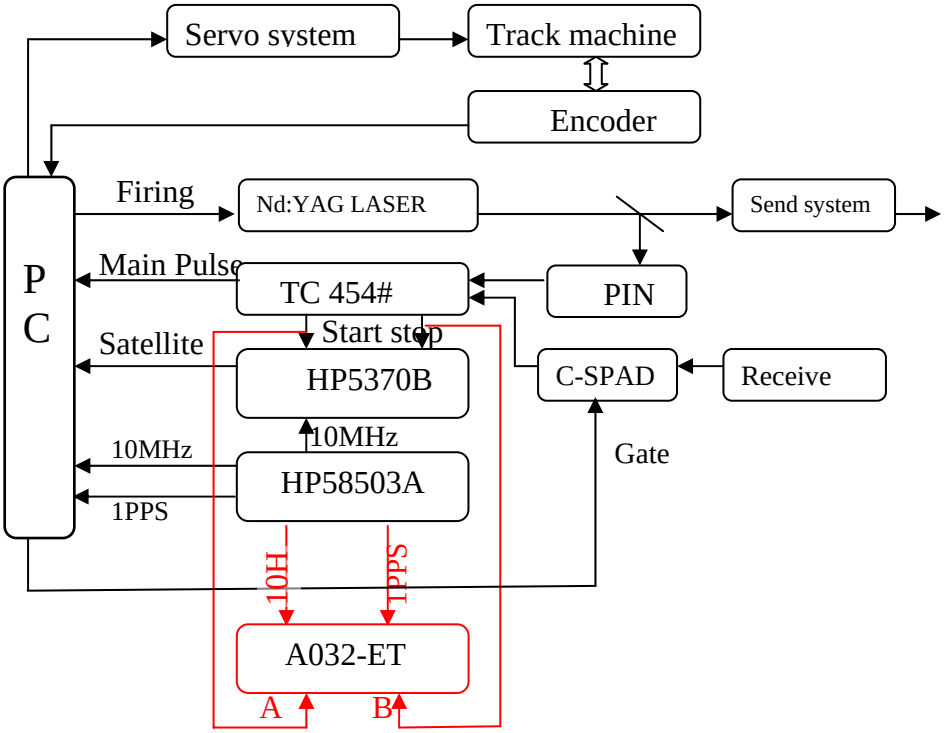


Figure 5. *Hardware connection*

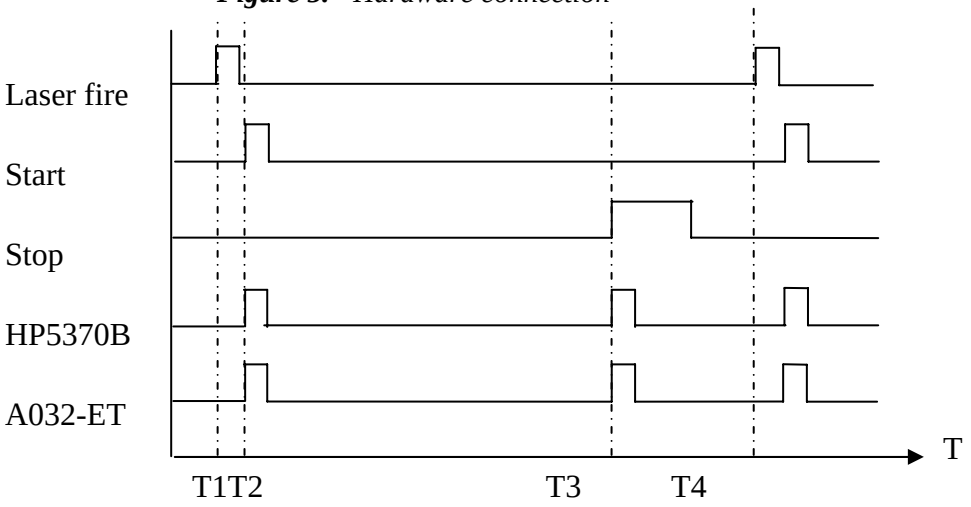


Figure 6. *Time sequence of Changchun SLR system*

Figure 7 shows the Etalon-2 measurement interface. The firing rate is 10Hz. From this picture, the return signal line can be clearly seen. From the satellite observation, we can see that the system works very well with A032-ET under the condition of 10Hz firing frequency. The return signal rate of high orbit satellites is increased.

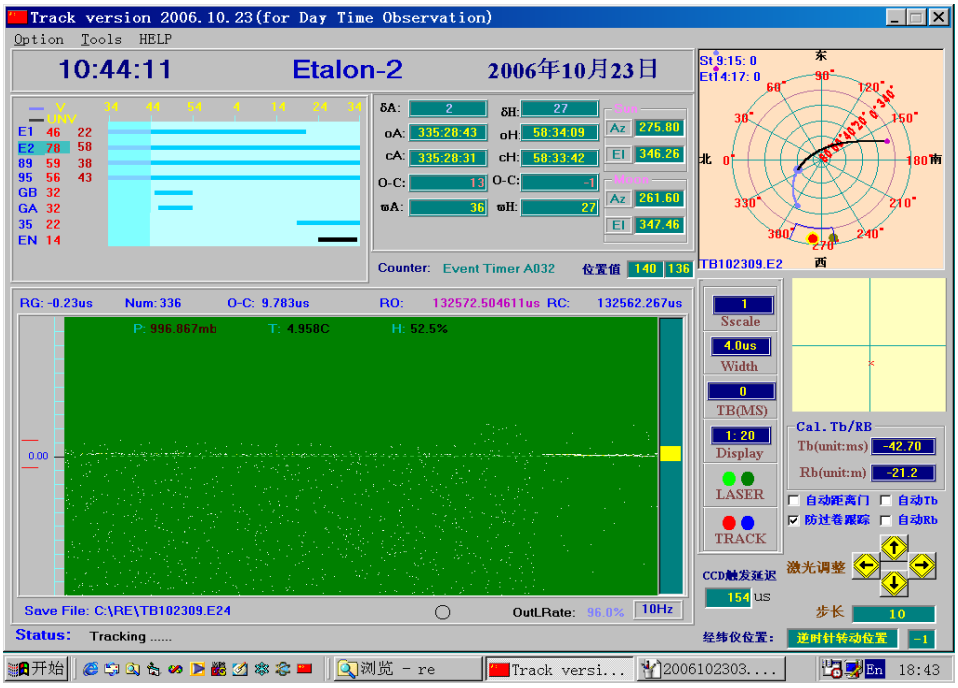


Figure 7. *Etalon-2 measurement interface*

Conclusion

From analysis report such as Toshi's report, we can see A032-ET works well as Event Timer. The precision is 1cm more or less. It could be used in SLR system normally. Because the laser pulse is about 200ps in Changchun station, the precision of the whole system does not increase obviously after the event timer is used. Since Oct.23 of 2006, A032-ET has been used in the satellite laser ranging routinely for the all satellites tracked with the firing frequency of 10Hz in Changchun station. Table 2 shows the data quantity from 2006-10-23 to 2006-12-31. There are too many passes. Now, it works very well and the experiment is very successful. Next, we plan to increase to KHz observation if the laser source is available.

Table 2: *Data of Changchun SLR Station (2006-10-23 to 2006-12-31)*

Site Information		Data Volume			
Column 1	2	3	4	5	6
Location	Station Number	LEO pass Tot	LAGEOS pass Tot	High pass Tot	Total passes
Changchun	7237	1095	153	209	1457

Acknowledgement

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Event Timing System for Riga SLR Station

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Abstract

The new Riga Event Timing System (RTS) is designed and built in 2006 for SLR station Riga-1884 to improve its measurement equipment in precision, functionality and reliability of operation. The RTS is a multimode instrument for satellite ranging at 10 Hz repetition rate with parallel measurement of PMT-pulse amplitudes for the range bias correction. The RTS can support millimetre accuracy of SLR although the overall system accuracy is limited by the other equipment of Riga SLR station. As compared to the previous version of Riga timing system, the RTS offers considerably better performance and functionality and provides a good basis for further improving the Riga SLR station as a whole.

Introduction

The Riga Event Timing System (RTS) is designed and built in 2006 for Riga SLR station to upgrade its measurement equipment. The RTS maintains the basic functional possibilities of the previous Riga timing system but is advanced in many essential respects. Specifically, the RTS is based on employment of the latest Riga Event Timer A032-ET [1]. As compared to the previously used instrument, the A032-ET provides much better single-shot resolution (8 ps RMS instead of the previous 25 ps) and much smaller “dead time” (60 ns instead of the previous 400 ns).

A new hardware design is made to integrate the most of specialized hardware means within a single stand-alone device. There are new functional possibilities of digital signal processing and system control that have to increase the SLR efficiency. Some optional functional capabilities are added for experimental investigations with the aim to improve the performance of Riga station as a whole.

A special feature of the RTS is that it provides pre-processing of STOP pulses coming from either traditional single or special doubled receiver based on Photo Multiplier Tubes (PMT). The doubled receiver generates the pulses overlapping only when the true STOP pulse is being received [2]. It makes possible to reduce the noise influence when the satellite ranging is performed by day. Like the previous Riga timing system, the RTS performs PMT pulse amplitude measurement to correct the range bias [3].

Principles of operation

The RTS supports the following operational modes:

- SLR system calibration in the range from 9 to 375 m with parallel measurement of STOP-pulse amplitudes;
- Satellite ranging to 25,500 km at 10 Hz repetition rate with parallel measurement of STOP-pulse amplitudes;
- Integrated mode when the SLR system calibration and satellite ranging are performed simultaneously (for optional use);
- Measurement of pulse noises.

Structurally the RTS combines the RTS hardware and a PC with the RTS software (Fig.1).

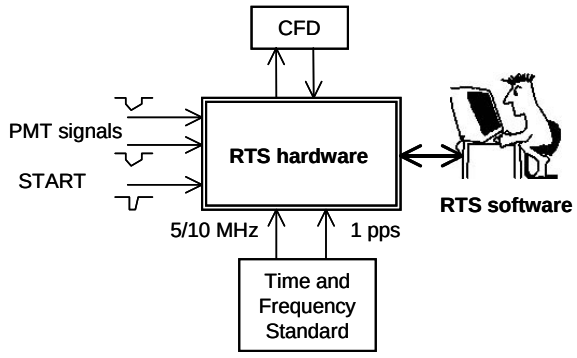

Figure 1. *RTS architecture*

Additionally the RTS includes two commonly used external devices: Time and Frequency Standard and Constant Fraction Discriminator (CFD).

The RTS hardware

The RTS hardware contains three functional units: Signal Processing block, Event Timer Block and Master Clock; each implemented as a separate board. These boards and their power supply are housed in 19'' 2U rack module (Fig.2).

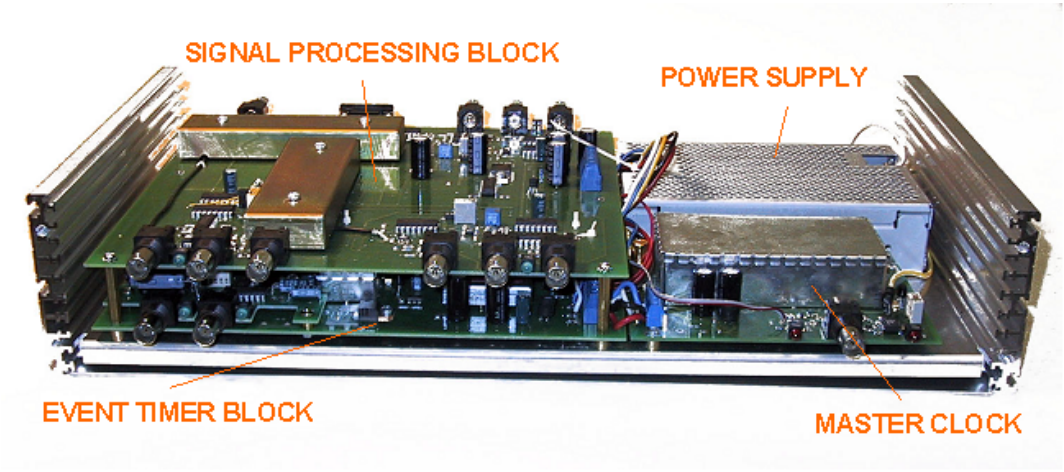

Figure 2. *RTS hardware assembly*

The Signal Processing Block receives the PMT pulses (3 to 7 ns width range; -0.1 to -3.0 V amplitude range) and, in interaction with the CFD, produces normalised NIM pulses for the Event Timer Block. The Event Timer Block measures time instants of these pulses and START pulses coming. Then the measurement results come to PC for further data processing, displaying and memorizing. The Master Clock represents a voltage-controlled crystal oscillator disciplined by an external high-stable 5 or 10 MHz reference frequency using PLL circuit. It generates a low-jittered 100 MHz clock signal required for precise event measurement and synchronization of Signal Processing Block operation as a whole.

Signal Processing Block

The Signal Processing Block performs a few basic operations with PMT pulses before their measurement by the Event Timer Block (Fig.3).

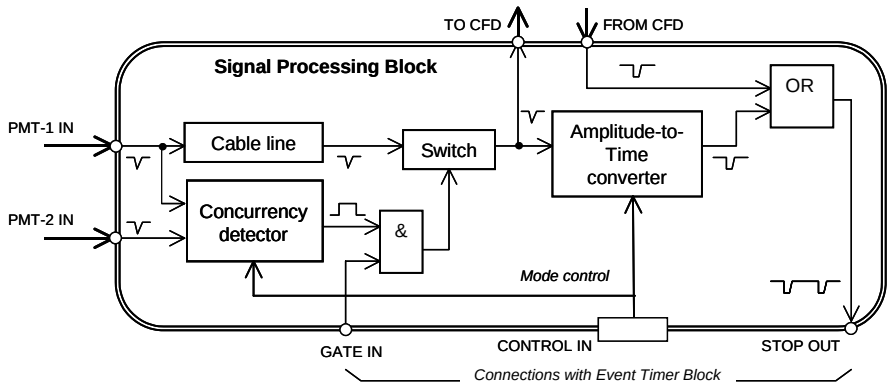

Figure 3. *Functional diagram of the Signal Processing Block*

At first it selects PMT pulses which probably conform only to the returned laser pulses. To do that either single ("PMT-1 IN") input or two ("PMT-1 IN" and "PMT-2 IN") inputs for PMT pulses can be used. In the last case it is supposed that the PMT pulses overlap only when the true return is being received. In the case of concurrency of these pulses one of them ("PMT-1") is selected using the wideband switch. Such selection acts together with the online programmable gating provided by the Event Timer Block.

The selected pulses from the switch output come to the CFD. The CFD generates normalized NIM pulse in response to each input PMT pulse. This NIM pulse comes to the input "FROM CFD" of the Signal Processing Block. However the CFD cannot fully avoid the time-uncertainty of PMT pulse coming. For this reason the amplitude of each PMT pulses is additionally measured as the amplitude values are related to the range bias. To do that, the Amplitude-to-Time converter generates the NIM pulse in response to the same PMT pulse with some delay proportional to the PMT pulse amplitude. In this way every selected PMT pulse is being converted into two NIM pulses where the first one represents directly the returned signal and time interval from the first pulse to the second one reflects its amplitude (Fig.4). Resolution of such amplitude measurement is about 9 bits.

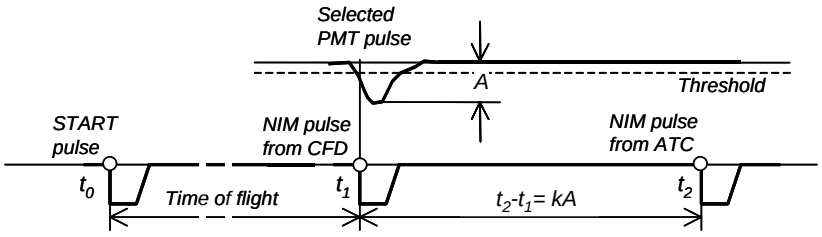

Figure 4. *Time diagram illustrating PMT pulse amplitude conversion*

Then the Event Timer Block measures time instants of these pulses and START pulse coming at each ranging cycle so as to give out complete data for further satellite ranging. As shown in [3], the mentioned technique of PMT signal amplitude measurement makes it possible to effectively correct the range bias caused by the PMT features.

Event Timer Block

The Event Timer Block precisely measures the instants at which input events occur. Every event is associated with certain fixed point on the leading edge of input NIM pulses. Used method of event timing is untraditional in many respects. Specifically, it

supports not only high precision but high speed as well. Using 100 MHz internal clocks this method provides each single measurement with 7-8 ps RMS resolution during 60 ns only.

The event measurement is performed in two stages. At first, the Event Timer Block transforms every input event into single 80-bit timing data block (subsequently referred to as TD-block) and sequentially accumulates them in a FIFO memory. Each TD-block contains the counting data (39 bits; 10 ns resolution) and interpolating data (40 bits), as well as one-bit mark specifying the kind of measured event (either Start or Stop). The interpolating data are presented initially in an intermediate redundant form.

At the next stage the PC takes out TD-blocks from the FIFO memory and processes them to obtain the corresponding epoch time-tags in a unified form. Further these time-tags are additionally processed to display the ranging results in real time. To achieve the best precision, processing of TD-blocks takes into account the actual physical characteristics of time interpolation under actual operating conditions; these characteristics are defined through so called scaling (hardware calibration) before the measurement.

The Event Timer Block is flexibly controllable and allows writing TD-blocks in the FIFO memory and reading them by the PC in different order. Specifically, the RTS provides cyclical measurement of events. In the beginning of each cycle the RTS measures a single Start-event, and only then - a number of Stop-events. According to the modes of RTS operation, the Event Timer Block measures up to 3 events in the System calibration and Satellite ranging modes, up to 5 events in the “Integrated mode” and up to 10000 events when pulse noise is measured. In all cases the Event Timer Block at first accumulates TD-blocks in the FIFO memory during some defined waiting period, starting from Start-event registration. During this time the PC processes TD-blocks that have been read out from the Event Timer Block in the previous cycle. Then the PC stops the event registration, reads the currently accumulated TD-blocks and allows starting the next similar cycle. The waiting period is strictly adapted to the repetition rate (10 Hz) of RTS operation. Optionally the RTS can provide the repetition rate up to 30 Hz.

In addition to the event measurement the Event Timer Block generates NIM pulses, which come to the input “GATE IN” of the Signal Processing Block to provide online programmable PMT pulse gating.

The RTS software

The RTS software performs real-time procedures which depend on the selected operating mode, current user control, etc. There are also various auxiliary procedures to prepare the system to operation (clock synchronization, calibration of measurement hardware, system checking, etc). For example, in the conventional Satellite ranging mode the RTS software performs in real time the following procedures:

- periodically checks the RTS hardware to detect the START pulse coming;
- when the START pulse is detected, triggers the internal time-out and begins processing of the previously taken data;
- when the time-out is finished, stops the measurement, reads the data from the RTS hardware, writes to it a new data concerning the STOP pulse gating and makes next cycle available.

Correspondingly the data processing performed during the time-out includes:

- conversion of TD-blocks to the unified form of epoch time-tags;

- calculation of the gate delay and residual, time interval reflected the STOP pulse amplitude and new data concerning the STOP pulse gating in the next cycle;
- displaying (Fig.5) and memorizing the measurement results.

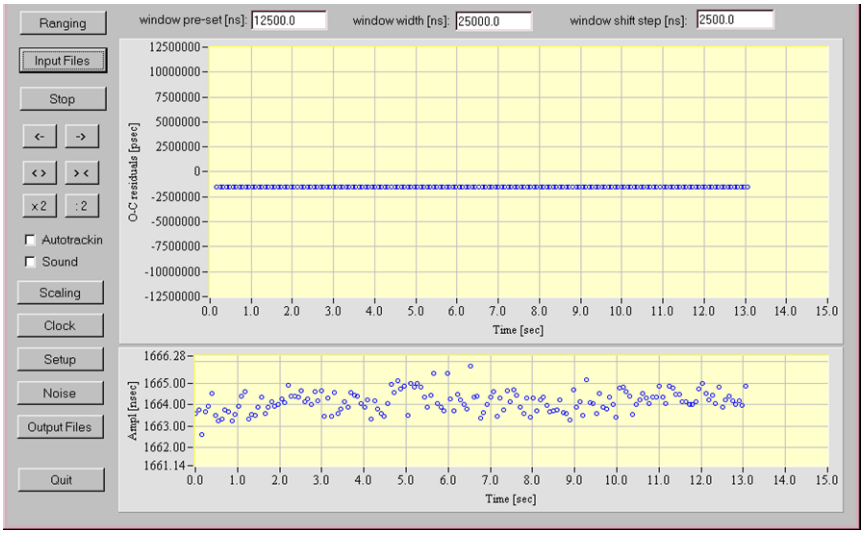

Figure 5. *Example of displaying the measurement results. Upper plot shows residuals; bottom plot indicates amplitudes of PMT pulses*

The RTS software offers optionally an autotracking of satellite in range after its initial acquisition. When the autotracking is on, possible trend of the residuals is actually excluded due to the automatic gate delay correction. Algorithm of the autotracking is based on median selection of current residuals to exclude their possible abnormal values, and continuous generation of a special piecewise-linear function for gate delay correction. Every piece of this function is being determined using regression analysis of the current fraction of residuals. In this case the gate delay correction is performed at 1 Hz rate approx., allowing considerable errors in initial predetermination of the function “RANGE vs. START TIME”.

The RTS software is written in *C* language for LabWindows/CVI ver.6.0 and works under Windows XP.

Conclusion

As compared to the previous version of Riga timing system, the RTS offers considerably better performance in terms of accuracy, functionality, and reliability in operation. This provides a good basis for further advancing the Riga SLR Station as a whole. In 2006 the RTS was involved in trial operation; the first series of successful SLR results has been obtained.

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Instrumentation for Creating KHz SLR Timing Systems

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Abstract

The instrumentation provides basic tools for creating SLR timing systems operating at repetition rate up to a few KHz. There is a test setup to simulate the process of ranging to various satellites and to evaluate capabilities of this instrumentation for the KHz system design. The simulation of the CHAMP laser ranging at 2 KHz repetition rate is considered as an example. Test results show that the proposed instrumentation offers sufficient performance to be used in the KHz SLR systems.

Timing system architecture

As known, increasing the SLR repetition rate up to KHz provides a variety of essential benefits. Currently there are a few SLR stations which already use this technique or will have it in the near future. However KHz SLR usually need essential upgrading of SLR equipment, including the timing system for satellite range measurement. In view of that we propose an instrumental basis to create various KHz SLR timing systems adapted to the specific user requirements.

There is the well-known custom timing system for KHz SLR at Graz SLR station [1]. In general terms, architecture of timing systems based on the proposed instrumentation and principles of their operation are similar. But there are distinctions in some essential details. Specifically, in our case the specialized hardware is offered as two compatible stand-alone devices (Event Timer A032-ET and Range Gate Generator). PC interacts with these devices and coordinates their operation via standard parallel ports working in the EPP (Enhanced Parallel Port) mode (Fig.1).

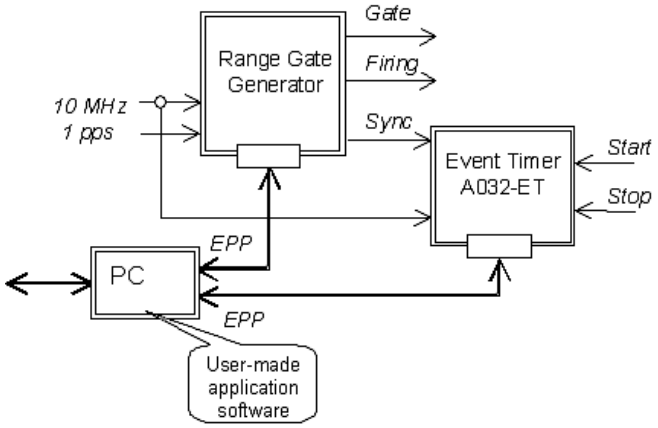

Figure 1. *Timing system architecture*

As for the application software, it should be custom-made according to the specific application requirements with the reference to the sample program (source code written in *C*). This program defines device-specific software functions which can be directly built in the user software to support the interactions with hardware. In this way the instrumentation can be used as a basis for various timing system designs.

System hardware

Event Timer

The basic system hardware component is Riga Event Timer A032-ET. It offers two independent inputs for *Start* and *Stop* measurement with RMS resolution about 7-8 ps. Distinctive feature of this device is exceptionally small "dead time" (60 ns) due to the advanced interpolating technique of event timing. This allows sequential measurement of *Start* and *Stop* using simple single-channel hardware structure (Fig.2). Note that such solution simplifies the timer's implementation and makes it relatively inexpensive.

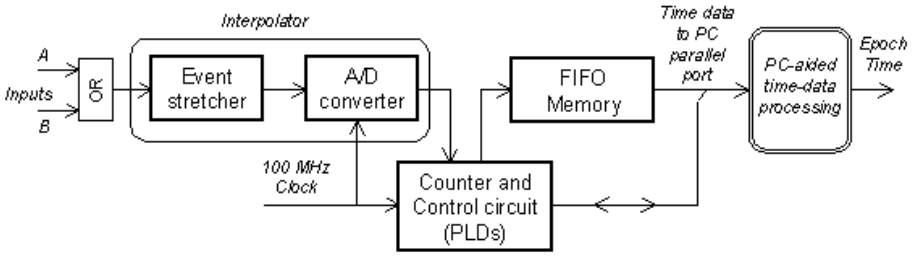

Figure 2. *Schematic block diagram of the Event Timer*

Although small "dead time" allows the burst rate of event timing up to 17 MHz (for up to 12K sequential events), the average rate is limited down to 10-15 KHz by the available speed of data transfer to PC. However it seems that this rate is quite enough for KHz SLR. In more details the A032-ET features are described in [2].

Range Gate Generator

The Range Gate Generator (RGG) is based on the well-known scheme of Digit-to-Event conversion (Fig.3). Continuous counting of 100 MHz clock pulses forms the 25-bit time-scale with 335 ms periodicity. Such periodicity directly conforms to the maximum value of range gate delay.

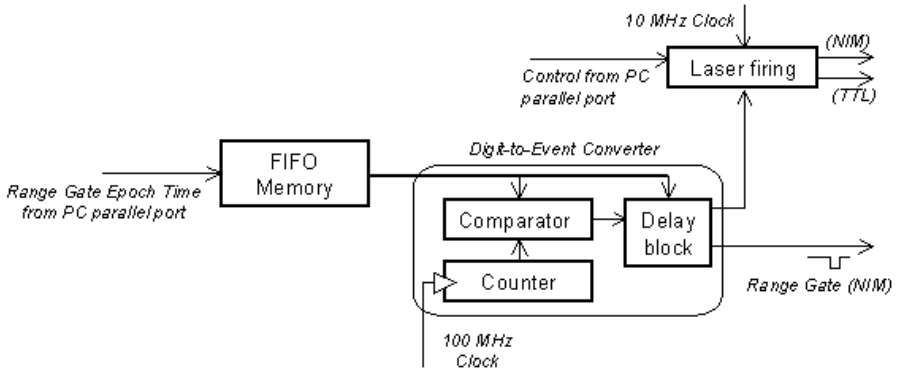

Figure 3. *Schematic block diagram of the Range Gate Generator*

Dual-ported FIFO memory receives the time data (Range Gate Epoch Time) from PC. In this case the data writing to this memory and data reading from it are independent asynchronous processes. Digital comparator compares the data from the FIFO memory with the current state of time-scale, providing the range gate generation with 10 ns resolution. Additional 7-bit controlled delay block (based on MC100EP196 delay chip) increases resolution up to 80 ps. However there is noticeable differential non-linearity for this chip, resulting in a noise-like error of range gate generation (80 ps RMS approx.). Most of the RGG digital functions are implemented on CPLD basis.

An important feature of the RGG is a specific firing generation. As known, the range measurement can be corrupted when a transmitted laser pulse is close to the received one. To avoid such problems each firing is generated so that it never can occur within some protected zone around any gate being generated (Fig.4).

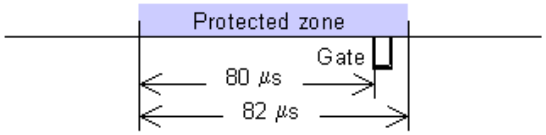

Figure 4. *Zone protected from firing*

To provide such condition, initially specified period of firings may sometimes be automatically (without any pre-calculations) incremented by quarter of its value. The nominal value of firing period can be set in the range from 100 μs to 167 ms with 0.64 μs resolution. In other words, the timing system is able to operate in a wide range of repetition rate, starting from 6 Hz.

Generally the RGG has been designed not only for KHz SLR applications. For this reason it also provides some additional features that are beyond of the direct KHz SLR needs. Specifically, it offers FIFO memory depth up to 16,000 data blocks defining the epoch times, cyclical offline operation, has two selectable outputs for two-channel event generation, etc. These features may be useful for other applications such as tests of timing devices.

General performance limitation

In the process of *Stop* gating each *Start* brings about corresponding control data at the RGG interface with some delay called “response time”. The response time is a system parameter that defines both the SLR maximum repetition rate and allowable minimum of satellite range.

There are three main components of the response time: time of data reading from the Event Timer, time of data processing and time of data writing to RGG. Usually it is desirable to dedicate the maximum time for real-time data processing. Correspondingly the total time of data reading (10 Bytes) and data writing (5 Bytes) via PC parallel ports (see Fig.1) has to be reduced as far as possible. Although formally the EPP should provide the data transfer rate up to 1-2 MB/s, actually it considerably depends on the PC operating system and its configuration. Specifically, our experiments with different MS-Windows operating systems showed that the total time of data reading/writing on average varies from 25 μs (for Windows-98) to 150 μs (for Windows XP). Furthermore, this time is not stable, resulting in significant variation of the response time from cycle to cycle. Unfortunately it was not possible to check other operating systems that could be better suited for real-time operation.

Experimental evaluation of system potentialities

To evaluate the potential of the proposed instrumentation a test setup has been used. This test setup has a structure which is similar to that shown in Fig.1. In this case each firing simulates *Start* and each generated gate simulates *Stop* for the Event Timer. Correspondingly a test program simulates application software. The test program performs the simplest real-time data processing related mainly to the Range Gate Epoch Time calculation and memorizing of the measurement results (no time-consuming operations such as real-time data displaying). Evaluation of the

measurement results is performed offline. The test program works under Windows XP. In this case the average response time was about 250 μs and its maximum value - about 1 ms. Most of the response time was consumed for the data reading/writing. These timing conditions correspond to the possibility of satellite ranging from 1 ms at repetition rate up to 4 KHz.

Other experiments were related to simulations of LEO satellites laser ranging as this represents a worst case for the timing system operation in possible real applications (the higher orbit, the less problems with the response time limitations). Specifically, the simulation of the CHAMP laser ranging at 2 KHz repetition rate was performed (Fig.5). There are 550,000 sequential readings obtained continuously during 275 seconds of the CHAMP pass simulation. The satellite range is from 2.45 ms up to 7.48 ms.

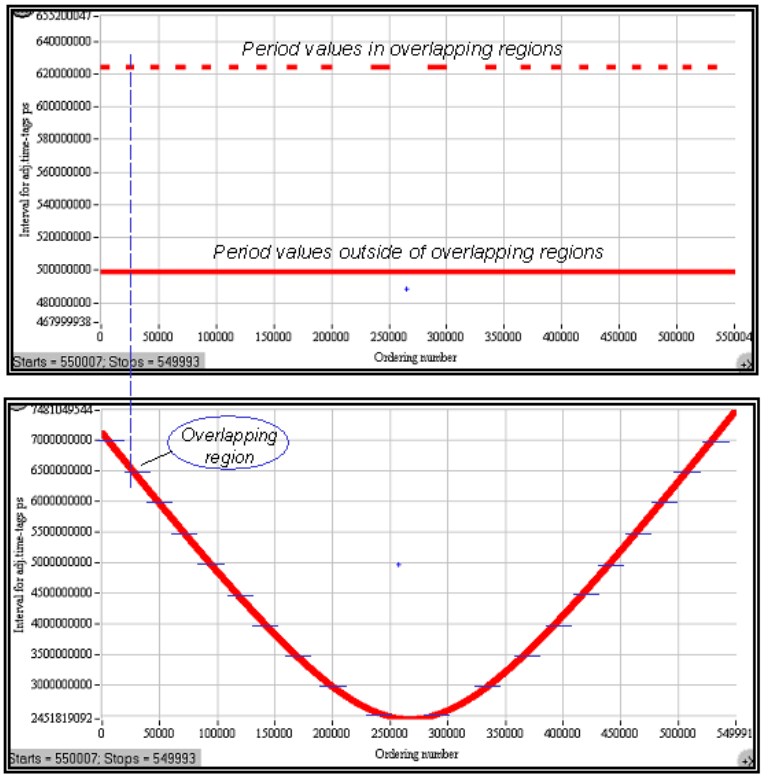

Figure 5. *Period of laser firing (upper graph) and measured range (in bottom) vs. cycle number for CHAMP laser ranging simulation*

As can be seen from the simulation result, there are a number of regions where the transmitting and receiving of laser pulses may overlap. Although the nominal value of repetition period was 499.2 μs, the actual average period was increased up to 502.157 μs (by 0.59%) due to incrementing of some firing periods (~2.4% of total number) by 0.125 ms to avoid these overlaps. Under these conditions any distortions or gaps in the measurement process were not detected. However, it should be taken into account that actually the real-time data processing can be much more complicated than that for the test setup. For this reason it is preferable to use the real-time operating systems to ensure the necessary time for data processing.

Additionally the residuals have been calculated to evaluate the system instrumental errors. When the Range Gate Epoch Times are defined for RGG with the maximum resolution (80 ps), there is a maximum non-linearity in the range gate generation (the

RGG interpolation delay varies in the full 10 ns range). Correspondingly in this case the calculated residuals reflect mainly the non-linearity errors of range gate generation (Fig.6). As can be seen, the peak-to-peak error is about 440 ps.

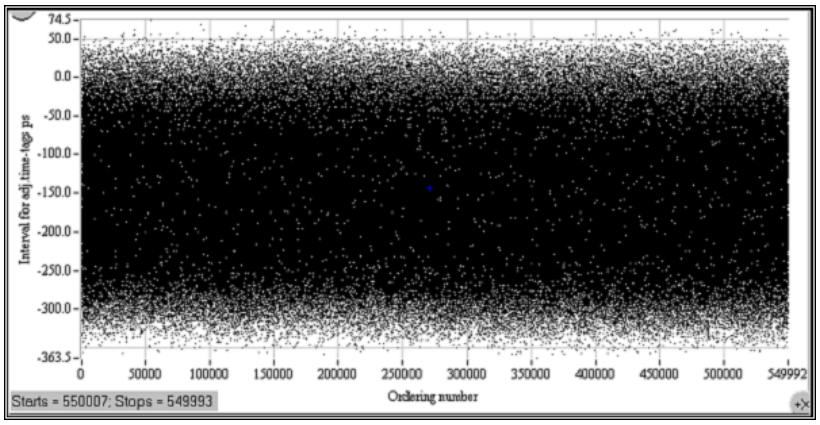

Figure 6. *Residuals vs. cycle number for CHAMP laser ranging simulation*

When the Range Gate Epoch Times are defined with 10 ns resolution, there is no noticeable non-linearity in range gate generation (since the RGG interpolation delay does not vary). Correspondingly in this case the residuals reflect both the errors of event timing and jitter of range gate generation. In our experiment the RMS of residual variation was about 8.9 ps. Since the actual RMS resolution of Event Timer is about 7.5 ps (this is specified by a separate test), it can be concluded that the RMS jitter of range gate generation is about 4.8 ps. Such jitter is negligible as compared to the actual RGG non-linearity.

Conclusion

We presume that KHz SLR is of vital interest for many SLR stations. Taking that into account, the proposed instrumentation offers sufficient performance for such applications and can be useful for creating new timing systems that provide SLR at repetition rate up to a few KHz. In this case the problems of timing system design can be reduced down to the development of user-specific application software.

Special thanks to Dr. Kirchner for his assistance and promotion of our latest designs. His well-known achievements concerning the KHz SLR at Graz station in many respects stimulated our activity in this area.

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OCA Event Timer

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Abstract

In the framework of T2L2[1,2,3] project, OCA and CNES designed an ultra stable event timer[4]. It includes on a unique card, a vernier, a logic counter, a 100 MHz frequency synthesis and a module for communications and internal calibrations. It has a precision better than 2 ps, linearity below 1 ps and a thermal drift in the range of 0.5 ps per degree. The dead time between two consecutive events is 3 µs.

For the T2L2 ground operations both the start time and the return time of laser pulses are required and not only the differences between the events. In order to run properly the T2L2 project, it will be necessary to upgrade some of the laser stations in that way. A T2L2 questionnaire was sent to the ILRS community to identify precisely the needs of each station.

For these reasons it has been decided to develop from the studies of the space design an event timer dedicated for ground operations. It could have the same characteristics than the flight model even if it seems possible to increase the frequency of the vernier to reach a sub picosecond precision and to decrease the dead time below 1 µs.

Introduction

An event timer is a system able to get the time position of an event in the time scale of a clock. It can be consider as a counter driven by the clock which is the time reference. When an event occurs, the value of the counter is extracted and this value represents the arrival time of the event. The time origin of such an event timer has to be measured with a reference signal like a PPS. A time interval is computed from the difference between two arrival times. The most important characteristics of an event timer are: the precision, the linearity, the time stability and the dead time.

Ideally, the linearity error has to be good enough so that the precision of the timer do not rely on the position of the event in the time scale produced by the clock. A precision of few picoseconds requires then a linearity error in the range of one picosecond. The time stability $\sigma_x(\tau)$ permits to evaluate the performances of the instrument when the events are acquired during τ. In the framework of the laser ranging activities, this is an important characteristic to construct the normal point. In the frame of the time transfer this important to evaluate the noise introduce by the timer as compared to the noise introduce by the clocks. The start time and the arrival time can be measured from the same event timer if the dead time between two consecutive measurements is small enough. A dead time in the range of 3 µs permits to range ground targets at 500 m. This is a minimum requirement to be able to calibrate a laser station with an external ground target.

A first breadboard of the T2L2 space instrumentation was built at OCA in 2002. Since then, T2L2 project was accepted by CNES on the satellite Jason2. We started the development of the space instrumentation in mid 2005. Three models were built: a prototype, an engineering model and the flight model. The flight model is now ready

to be integrated on the satellite.

Description of the T2L2 event timer

The event timer is made with 4 distinct modules on a unique card (figure 1):

- A vernier having a time resolution of 0.1 ps
- Frequency synthesis @ 100 MHz controlled from an external 10 MHz clock signal coming from the DORIS system.
- Calibration module to improve the long term time stability
- Digital module for communication through a RS422 serial bus

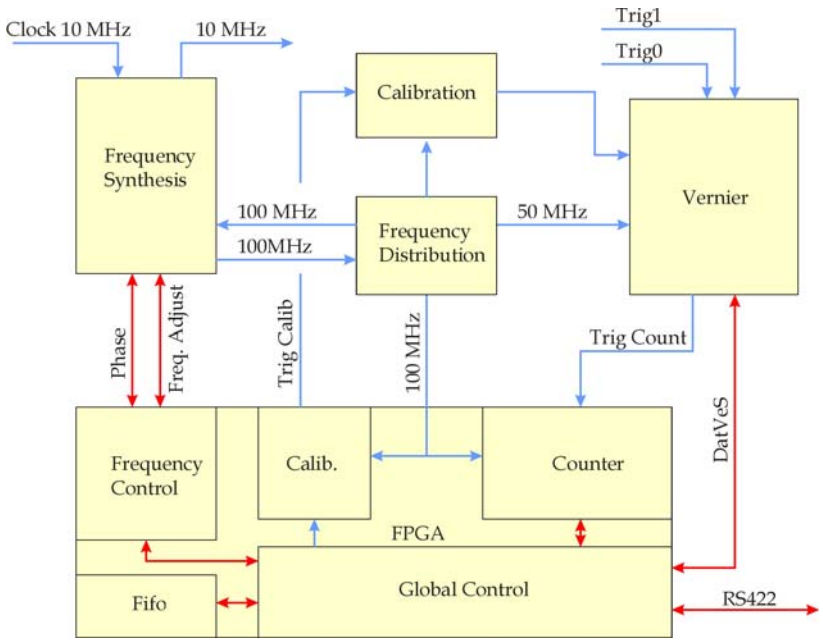

Figure 1 : *Synoptic of the event timer.*

The most important module is the vernier which give the arrival time of the event with a resolution of 0.1 ps. It is driven by the digital frequency synthesis module designed to translate the 10 MHz clock signal to 50 and 100 MHz. The global performances of the timer rely on these two modules. The calibration module permits to improve the long-term stability of the timer. It generates calibrated events that are timed by the event timer. The frequency synthesis is built from an ultra low noise quartz oscillator @ 100 MHz (ArElectronic) controlled with a Phase Lock Loop based on a digital phase measurement. Figure 2 gives the time stability specification of both the DORIS Oscillator and the ArElectronic oscillator. The PLL is tuned to get a frequency cut at 100 Hz with a damping factor of 3. The digital module is divided in 2 parts. The first one is a digital counter driven by the frequency synthesis signal. It gives the arrival time of the event with a time resolution equal to the period of this signal: 10 ns. The second one is the global control of the timer. It controls all the modules and the serial bus.

The complete T2L2 space instrument includes four more cards, two for the detection, one for the computer and memory and one for the power supply. It also includes an optical module made with an avalanche photodiode provided by PESO [5]. All these modules are gathered in a compact aluminium box (figure 3), which is placed inside the satellite payload. The instrument is completed with a detection module located

outside the satellite and very close to the Laser Ranging Array provided by ITE inc.

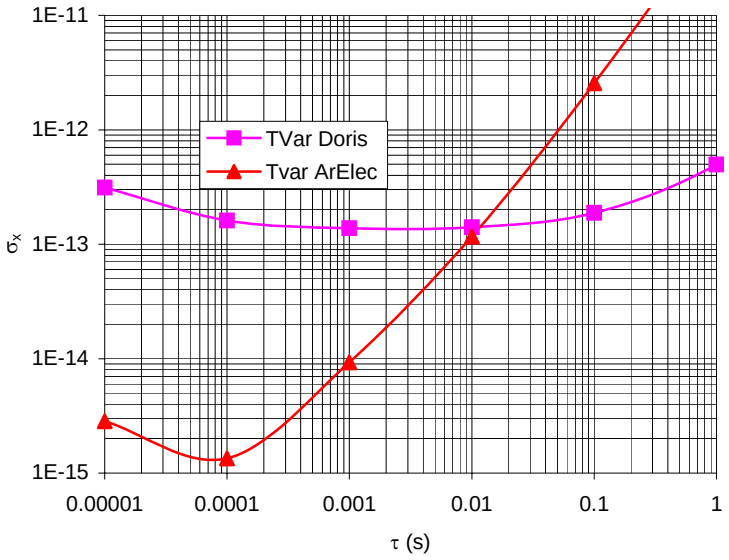

Figure 2 : *Time stability of both the local oscillator and the external oscillator*

The global characteristics of the event timer are:

Input frequency	10 MHz sinus 0 dBm
Event input	2 inputs, ECL level
Local oscillator	100 MHz; noise floor : -165 dBc
Logical frequency	100 MHz
Dynamic	5.7 years
Vernier period	20 ns
Vernier resolution	0.1 ps
Vernier precision	< 2 ps rms
Vernier linearity	< 1 ps rms
Vernier Time Stability	< 30 fs over 1000 s
Vernier Thermal sensitivity	< 1 ps/°C
Vernier Magnetic field sensitivity	< 1ps /100 µT
Calibration Precision	0.9 ps rms
Freq synthesis stability	$\sigma_x = 0.2 \times 10^{-12}\ \tau^{-1/2}$ s @ τ0 = 40 ms
Communication	RS422 @ 1 Mbits
Continuous rate	7000 Hz
Dead time	3 µs
Memory	2 frames
Size	220 x 180 mm²
Power consumption	15 W

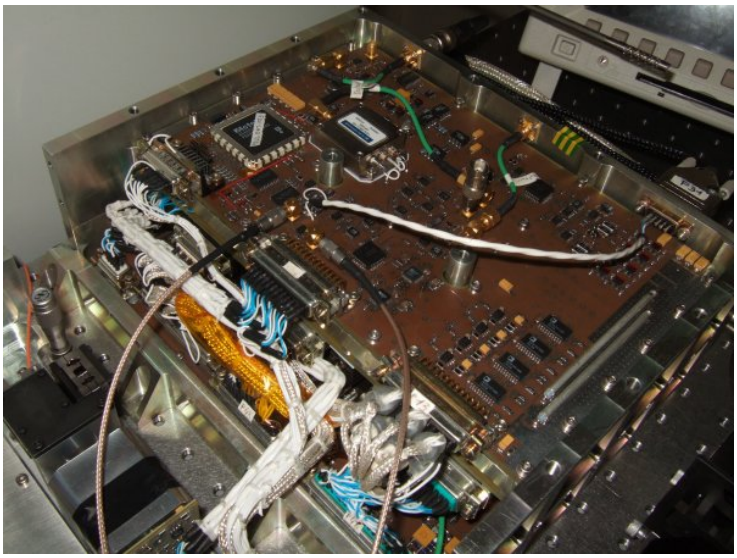

Figure 3 : *T2L2 Electronic instrumentation. The electronic card (in the center of the photography) is the event timer. A part of the Geiger photo detector can be seen on the left side.*

T2L2 ground instrumentation

For the T2L2 ground operations, both the start time and the return time of laser pulses are required and not only the differences between the events. In order for the T2L2 project to run properly, it will be necessary to upgrade laser stations in that way. A T2L2 questionnaire has been sent to the ILRS community to identify precisely the needs of each station. The questionnaire will help us to define the specifications and the design of the event timer: communication, size, number of entry, input frequency, etc.The event timer designed for T2L2 is not dedicated for T2L2: it will also be perfectly well suited for laser ranging. The timer could have the same characteristics than the flight model even if it seems possible to increase the frequency of the vernier to reach a sub picosecond precision and to decrease the dead time below 1 µs.

Conclusions

With an expected improvement of one order of magnitude as compared to existing time transfer techniques, T2L2 will allow the calibration of various existing radiofrequency time and frequency transfer systems like GPS or TWSTFT, and comparisons of cold atomic clocks at a level never reached before. Both the characterizations of the engineering model and the first measurement of the flight model allow us to be confident about the whole performances of the project. The T2L2 space model could also be used in the future in the framework of some interplanetary projects like TIPO [6] (One way laser ranging in the solar system) and Astrod [7] (Astrodynamical Space Test of relativity using optical devices) or LATOR.

Figure 4 : *laser ranging network : Event timer status in September 2006. In yellow laser station requiring an upgrade ; in green, compatible laser station (from the questionnaire)*

For a ground application, the performances of the event timer are at least one order of magnitude better than the performances of the other sensitive elements in the chain: laser – photo-detection. The short dead time between two consecutive measurements (that could be below 1 µs for the ground design) could permit to envision a laser station with only one timer and one photo detection system that will allow a direct accurate laser ranging measurement without any external calibration.

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The Model A032-ET of Riga Event Timers

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Abstract

The Event Timer A032-ET is an advanced version of the earlier model A031-ET of Riga event timers. As compared to this model, the A032-ET offers better single-shot resolution (<10 ps RMS) and is adapted to KHz SLR, supporting continuous measurement at the mean rate up to 10 KHz. At the same time it satisfies basic demands of conventional (low-rate) SLR. In this paper the principles of operation and basic features of the A032-ET are considered. Typical test results concerning the evaluation of single-shot resolution, linearity and offset drift are presented.

Introduction

Riga Event Timer A032-ET was designed in 2005 as an advanced version of the previous model A031-ET [1] with the main aim to adapt it to KHz SLR and improve its operating characteristics. As a result the following additional features of the A032-ET have been achieved:

- Continuous measurement at mean rate up to 10 KHz;
- Client-Server interaction supporting full remote control from the Client;
- Increased single-shot resolution (better than 10 ps RMS);
- Decreased "dead time" (not more than 60 ns);
- Built-in online programmable Stop pulse gating.

At the same time the A032-ET satisfies basic demands of conventional SLR at repetition rate up to tens of Hz and remains affordable at price. A032-ET is already known for some part of users. In particular, during one year after its designing about 10 instruments were delivered to different SLR stations. In this paper the principles of operation and basic features of the A032-ET are considered in more detail.

A032-ET main features

The A032-ET is a computer-based instrument that precisely measures epoch times when events (input pulse comings) occur. There are two alternative modes of the A032-ET operation that are tailored to the high-rate SLR and conventional low-rate SLR respectively:

- **"True Timer"** provides continuous (gapless) measurement of events at high (up to 10 KHz) mean measurement rate, allowing bursts up to 16 MHz. This mode suits well to measure Start and Stop events that come at the separate inputs (either *A* or *B*) of the A032-ET in any order.
- **"Multi-Stop Counter"** provides cyclical measurement of events that come at the separate inputs of the A032-ET in the strict order: in every cycle at first the A032-ET measures a single Start event coming at the input *A*, and then – a user-defined number of Stop events (up to 12,000) coming at the input *B*. The Stop events can be measured with online programmable gate delay.

Such measurements are performed with 7-9 ps RMS resolution in practically unlimited range. Extreme low measurement non-linearity (<1 ps) is supported.

A032-ET architecture

Like the most of virtual instruments, the A032-ET performs its measurement functions partly by hardware means and partly by software means. The measurement software provides interfacing with a user program via TCP/IP based network according to the well-known “Client/Server” scheme. The application program using TCP/IP service utilities can control the A032-ET and receive measurement data from it for further specific-application processing.

In terms of the Client/Server architecture the A032-ET can be considered as a combination of a specialised timing device (ET-device), and a specialised Server (ET-server) dedicated both to managing the ET-device and primary processing the timing data obtained from it (Fig.1).

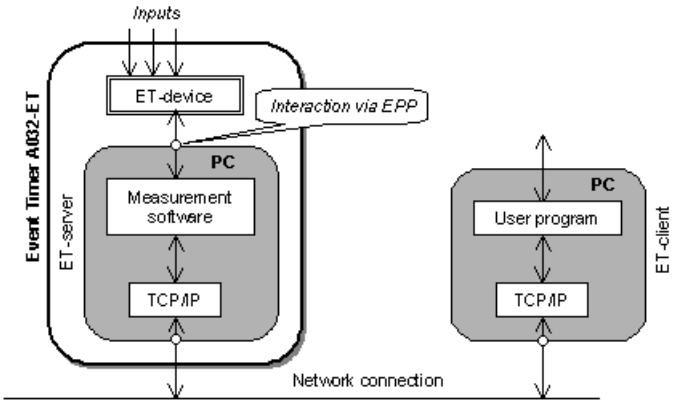

Figure 1. *Network architecture of the Event Timer*

In this case the ET-client is a PC on which user runs his application, using the specific ET-server resources via network. In many cases a single PC under MS-Windows can serve as both the ET-server and the ET-client although a separate PC for the ET-server is preferable to achieve the highest operating speed.

Principles of operation

The A032-ET performs the measurement of input events in two stages. At first, the ET-device transforms every input event into single 80-bit timing data block (TD-block) and sequentially accumulates such blocks in a buffer FIFO memory. Each TD-block contains the clock counter data (39 bits) and interpolating data (40 bits) about the time of event incoming, as well as one-bit mark specifying the input (either *A* or *B*) providing the measured event. The interpolating data are presented initially in an intermediate redundant form and need further an additional processing by the ET-server.

The used unconventional method of event timing supports both high precision and high speed. Specifically, using the 100 MHz internal clocks the method provides each single measurement with <10 ps RMS resolution during 60 ns only. This gives the maximum available rate of event timing about 16 MHz. At this rate the applied FIFO memory is able to accumulate up to 12,000 TD-blocks. An additional attractive feature of this event timing method is that it leads to the relative simplicity of hardware implementation (Fig.2). At the next stage the ET-server reads TD-blocks from the FIFO memory and processes them to obtain the corresponding time-tags in a unified form. Further these time-tags are sent to the ET-client via network.

The ET-device is flexibly controllable and applies two different procedures of TD-

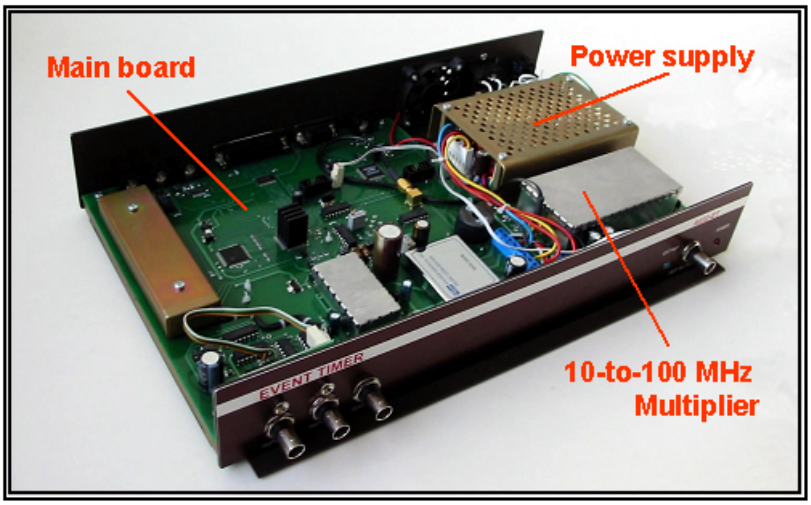

Figure 2. *Hardware design*

block accumulation in the FIFO memory and TD-block reading by the ET-server for two operation modes respectively

In the **"True Timer"** mode the ET-device provides continuous event measurement during practically unlimited time. To do that, the ET-device continuously accumulates TD-blocks in FIFO memory in order of measured event incoming. Concurrently with this process, the ET-server continuously monitors the current state of the FIFO memory with some user-defined period to detect the state when the amount of TD-blocks exceeds the user-selectable value (204, 102, 50, or 25 TD-blocks). The rest of the FIFO memory capacity is used to damp possible bursts of input event intensity. When the specified FIFO state is detected, the ET-server takes out the defined amount of TD-blocks from the ET-device, processes them and sends the corresponding time-tags to the ET-client. Such procedure is being cyclically repeated. In this way continuous event registration goes together with cyclical timing data processing and sending the time-tags to the ET-client via network. The mean rate of such continuous measurement is limited mainly by the available speed of TD-block reading and processing by the PC of the ET-server. Typically (although it may depend on the actual performance of the PC) the total time of single TD-block reading and processing on average is about 0.1 ms, resulting in the maximum mean measurement rate about 10 KHz.

In the **"Multi-Stop Counter"** mode the ET-device provides cyclical measurement of events. In the beginning of each cycle the A032-ET measures a single Start-event coming at the Input *A* of the ET-device, and only then - a number of Stop-events (up to 12,000) coming at the Input *B*. In this case the ET-device accumulates TD-blocks in the FIFO memory during some user-defined waiting period, starting from Start-event registration. During this time the ET-server processes TD-blocks, which are read from the ET-device in previous cycle, and sends the corresponding time-tags to the ET-client. Then the ET-server stops the event registration, reads the accumulated TD-blocks (but not more than the user-defined amount) and starts the next similar cycle. The waiting period can be defined in a wide range with a 1 ms step.

During the waiting period the ET-server can receive a command from the ET-client to restart the measurement with modified gate delay. In this way online cycle-to-cycle controllable gating is possible. However it should be taken into account that the real network may produce some unexpected delays for data exchange, resulting in

episodic loss of synchronism in such interactive operation at a high (more than tens of Hz) repetition rate of measurement cycles.

Precision characteristics

Although, in fact, the A032-ET measures the separate events, its precision is specified for time interval between two measured events. In this case the total measurement error ΔT_j for time interval T_j represented by difference of any two time-tags can be expressed as follows:

$$\Delta T_j = B(t) + E(T_j) + \xi_j,$$

where:

$B(t)$ – time-varying offset in measurement;

$E(T_j)$ – non-linearity error that depends on the value of measured time interval;

ξ_j – unbiased random error.

Specific values of these components of measurement error are evaluated for each instrument. Let's consider some typical examples of such evaluations.

Single shot RMS resolution

The A032-ET provides the best RMS resolution (standard deviation of the error ξ_j) directly after ET-device calibration. Then the resolution may slightly degrade under time-varying temperature conditions (Fig.3).

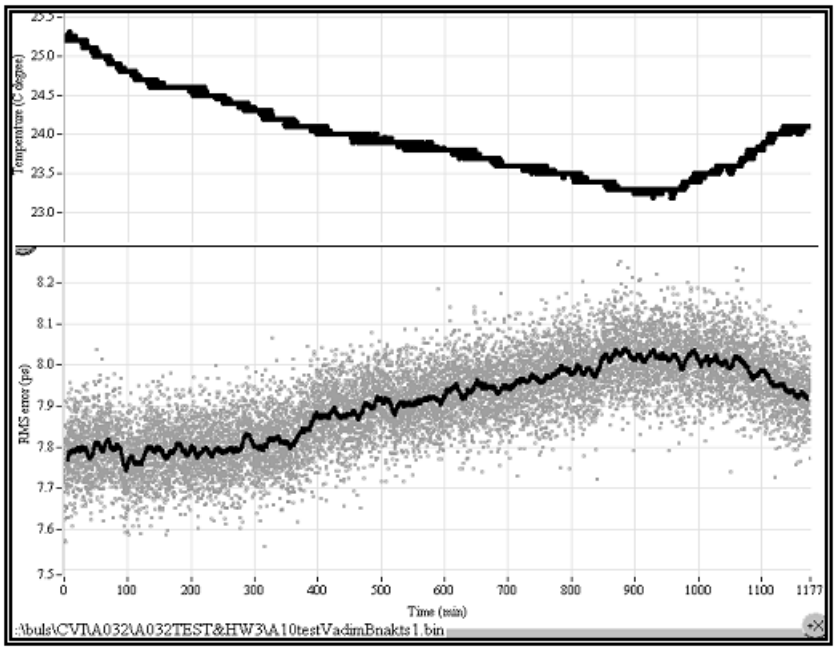

Figure 3. *Ambient-temperature and RMS resolution vs. time*

As can be seen, initially the RMS resolution is about 7.8 ps. During the next 15 hours the ambient-temperature is gradually changed for 2°C, resulting in decreasing of the RMS resolution down to 8 ps (about 0.1 ps/°C).

Linearity

There is some damping transient in electrical circuits responsible for event measurement. If such transient is not completed by the beginning of the following measurement it will be performed with some error. This error depends on the time interval between previous event and event currently measured, causing non-linearity in event measurement.

The A032-ET corrects such non-linearity but cannot exclude it completely, leaving slight, noise-like residual non-linearity in the range up to 2000 ns. This non-linearity appears as errors, which are particular and constant for every 1 ns step of time interval incrementing (Fig.4). In the range exceeding 2000 ns the non-linearity is negligible.

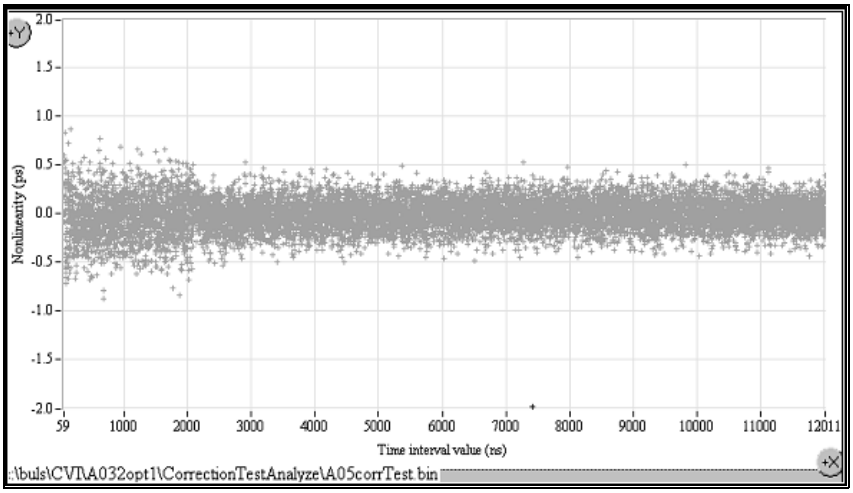

Figure 4. *Typical result of non-linearity error testing*

As can be seen, the maximum non-linearity does not exceed ±1 ps. However such estimate is overstated by reason of the additive evaluation errors (these errors are directly present in the range from 2000 ns). Actually the non-linearity is much smaller.

Offset drift

All events coming at either input of the ET-device are measured sequentially in the same manner and by the same means. Owing to this there is no any noticeable offset in time intervals between measured events when these events come at the same input. However when the events come at the different inputs it results in some offset. The offset is caused by a difference between internal propagation delays of input signals before their coming to the common measurement unit. These delays slightly vary with the ambient-temperature change, thus causing certain offset drift and corresponding long-term instability in time interval measurements.

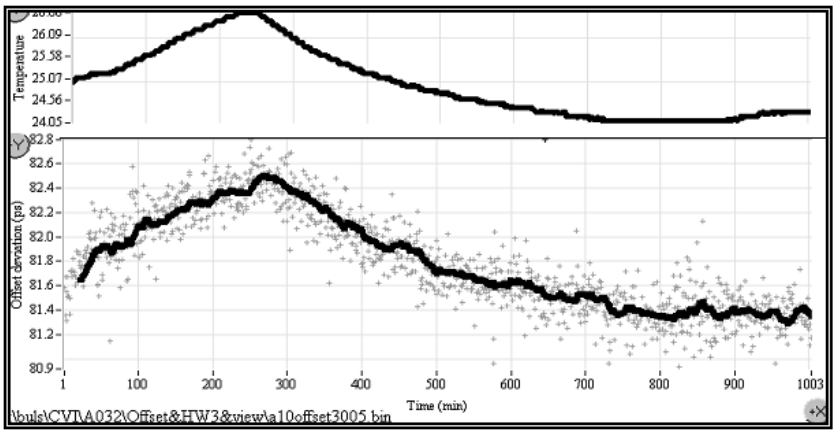

Figure 5. *Ambient-temperature and offset vs. time*

As can be seen from the example shown in Fig.5, the offset variation is directly related to the temperature variation, indicating in this case the offset temperature stability about 0.48 ps/°C. Generally this parameter value depends on the specific operating conditions.

A032-ET summary specification

Generalizing the test results that have been obtained at least for 15 units of the A032-ET, the following summary specification can be stated:

Inputs (BNC): INPUT A	NIM pulse (falling edge; >5 ns width)
INPUT B	NIM pulse (falling edge; >5 ns width)
SYNC IN	TTL pulse (rising edge, 1 pps)
TRIG IN	TTL pulse (rising edge)
REF IN	10 MHz (>0.5 V p-p)
Single-shot RMS resolution	<10 ps
Dead time	60 ns
Non-linearity error	<1 ps (<3-5 ps for time intervals less than 100 ns)
Offset temperature stability	<0.5 ps/^{0}C after warm-up
Warm-up time	2 hours
FIFO depth	12,000 time-tags
Measurement rate (True Timer)	up to 10 KHz continuously
Stop pulse gating (Multi-Stop Counter)	online programmable via network (10 ns LSD, 60 ns to 167 ms range)
Control	fully remote control from a user program via the network
Application interface	over TCP/IP
Hardware interface	via PC parallel port supporting EPP mode
Server software	MS-Windows based
Accessory software	DEMO application software
Hardware dimension, weight	375x60x233 mm (desktop); 3.0 kg
Power supply	100-240 VAC

It should be pointed that the A032-ET is a custom instrument manufactured in a limited quantity and only on request. For this reason such instruments may differ from one to another in some details. Additionally it should be taken into account that the measurement rate may depend on the actual performance of the user's PC and network.

Additional notices

The A032-ET is currently available in the following configuration:

- ET-device;
- Server software A032.1 that provides **"True Timer"** mode;
- Server software A032.2 that provides **"Multi-Stop Counter"** mode;
- DEMO Client software (including source codes in *C*) that illustrates the manner in which the user can create own specific application.

Optionally the Sample program (source code in *C*) is available. This program defines the device-specific software functions to communicate with the A032-ET hardware via PC Parallel Port. These functions can be directly built in the user software when the user desires to create fully integrated timing system.

References

[1] http://ilrs.gsfc.nasa.gov/docs/timing/Event-Timer-A031-ET.pdf

Upgrading of Integration of Time to Digit Converter on a Single FPGA

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Abstract

A Time to Digit Converter (TDC), which can achieve resolution 50-60 picoseconds, is integrated on a single FPGA. Implementing a TDC on an FPGA provides not only higher precision and shorter dead time compared to traditional methods, but also higher scale of integration. As the system can be integrated into single chip, it is especially suitable for portable and satellite-borne system. Besides, the resolution is expected to be improved to less than 30 picoseconds. Principle of operation, architecture of the prototype, the construction of this TDC and the nonlinearity are presented in this paper.

Introduction

Traditional high-precision time interval measurement techniques include time stretching method, time-to-amplitude method and Vernier method, tapped delay line method and differential delay line method [1]. There are two examples of TDC integration on a single FPGA: Jozef Kalisz *et al* adopted differential delay line method on QuickLogic's pASIC2 FPGA, which achieved 100 ps LSB [2]. Zielinski and Chaberski, using tapped delay line method, implemented a module on Xilinx's XCV300 with 100 ps resolution [3]. In this paper, a TDC is implemented on a XC4VSX35 FPGA with 50-60 picoseconds resolution. Table 1 lists main parameters of this module as below.

***Table 1**: Design Summary*

Standard uncertainty	50--60 picoseconds
Resolution/LSB	50--60 picoseconds (expected to reduce to 20-30)
Measurement Range	0-99999 seconds
Input Reference Clock	10MHz Rb Atom Clock
Calibration Mode	Real time Calibration

General Design

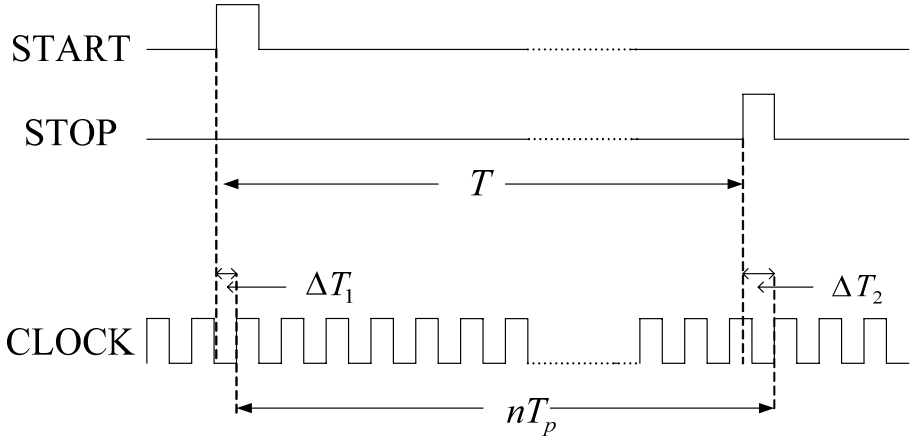
Interpolating Principle

Interpolating methods are widely used because of its advantages in both long measurement range and high resolution. With interpolating methods, a time interval T generally consists of three parts. A major part, nT_p, is measured in real time by reference clock. The remaining two short intervals ΔT_1 and ΔT_2 are defined at the beginning and at

the end of time interval *T*, which are measured by insulators. In this design, they are measured by two tapped delay lines. Fig. 1 gives the math relation between them.

Reference clock

The input 10MHz reference clock from Rb atom clock is quite stable but not high enough for interpolating. With built-in DCM on FPGA, it is synthesized into 200MHz. As shown in Fig.1, the time interval nT_p is counted by the reference clock 200MHz. The measurement jitter of 200MHz reference clock is about 60 picoseconds.



$$T = nT_p + \Delta T_1 - \Delta T_2$$

Figure 1. *Interpolating Principle*

Tapped Delay line

The tapped delay line is made of slices - the basic unit of the Virtex FPGA. As shown in Fig.2, a delay unit and a D flip-flop, is in the dashed line. The dashed part of delay logic can be implemented in a single slice, as shown in Fig. 3. These slices cascade to form a slice chain, i.e., a tapped delay line. Two delay lines of this kind, measure the short time interval ΔT_1 and ΔT_2 respectively.

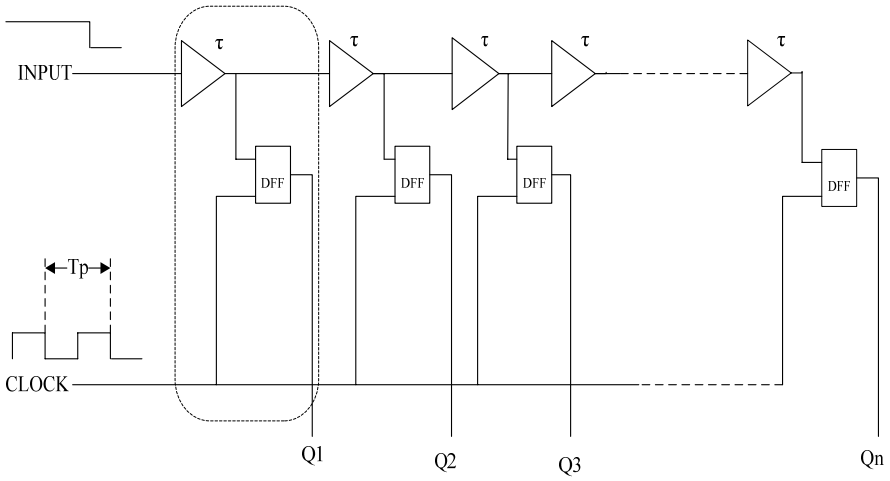


Figure 2. *Tapped delay line made of slices.*

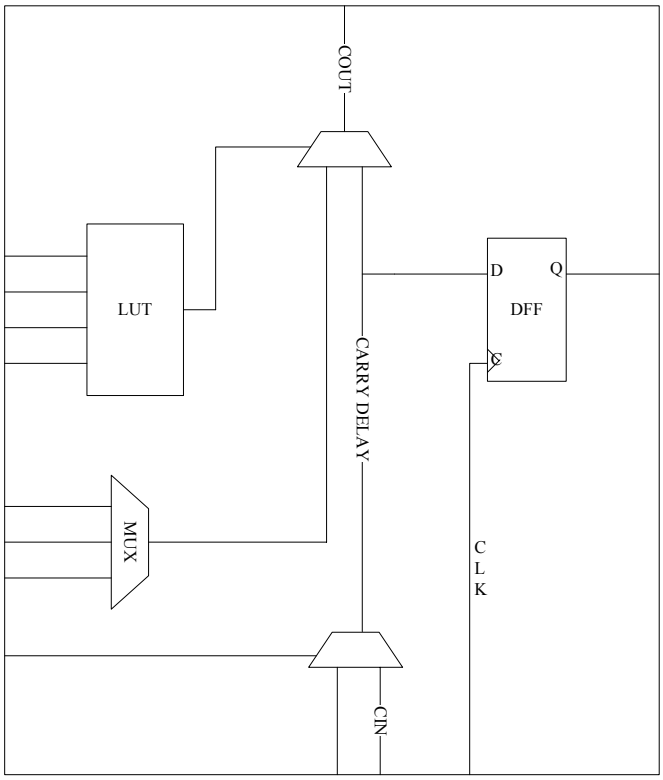


Figure 3. *Simplified slice configuration as delay unit.*

The delay unit of slice utilizes the fastest path, fast carry logic, to obtain the highest resolution. It's assumed that all delay units are of the same delay time τ. The measurement average delay τ, which determines the resolution or least significant bit of this module, is about 50-60 ps. However, this assumption does not fit the facts perfectly. The nonlinearity of the tapped delay line is measured and analyzed in the next part.

Measurement data

In this part, the measurement data of this module is compared with those of SRS's SR620. To demonstrate the resolution of this high-precision TDC, y axis of Fig 4 is marked with TDC measurement, while the x axis is marked with SR620 measurement.

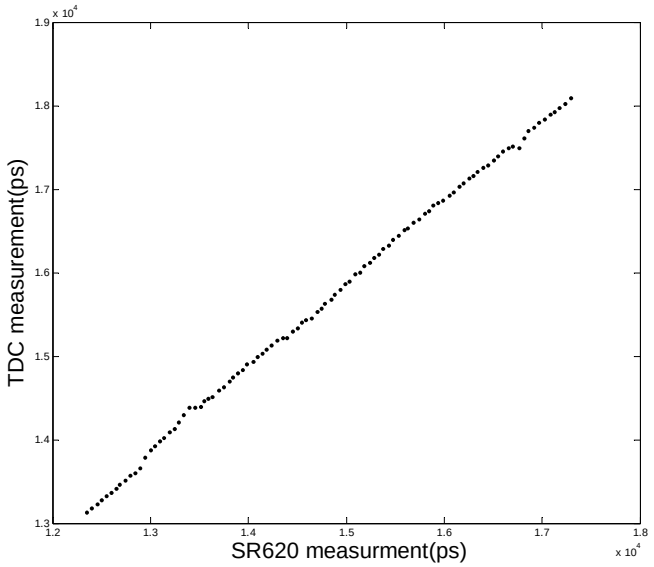


Figure 4*. Comparison of TDC measurement with SR620 measurement*

The difference between two groups of measurement, which is equal to the differential nonlinearity, is given in Fig. 5. In Fig.5, the maximum difference is about 300 picoseconds. The difference measurement can be repeated in other time cycle, which means it can be corrected with prior knowledge of it. This will be part of further research. Besides, with a little internal modification, the resolution is expected to reduce to less than 30 picoseconds, which means 50% improvement in resolution. This will be part of our future work.

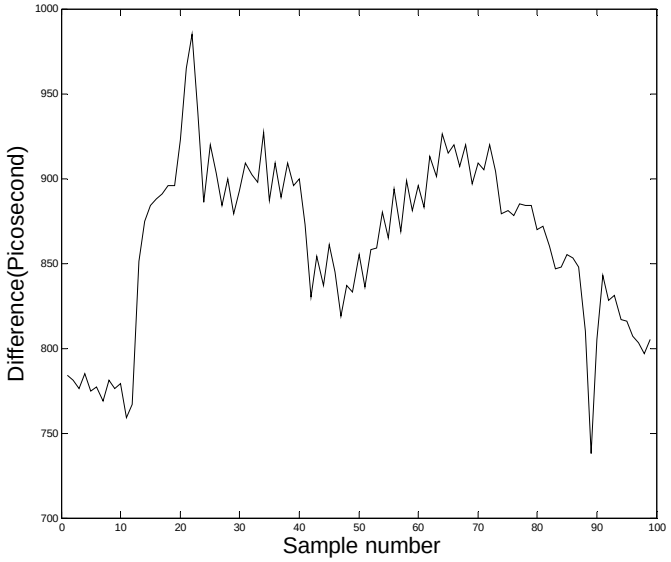


Figure 5. Difference between TDC and SR620

Fig.6 is a snapshot of our measurement experiment.

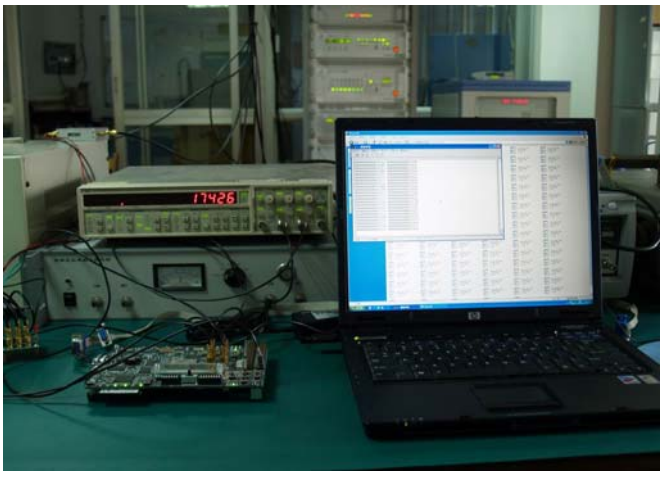


Figure 6. Measurement experiment

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[3] Zielinski M, Chaberski D., and Grzelak S., 2003. Time-interval measuring module with short dead-time Metrol. Meas. Syst. 10.

High-Speed Enhancement to HTSI Event Timer System

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Abstract

HTSI has developed a high-performance Event Timer Controller to pair with the HTSI Event Timer that allows acquisition of UTC tagged event epochs with <2ps jitter and 0.5ps resolution from up to 12 input event channels at continuous asynchronous event acquisition rates of over 50kHz. The increase in sustainable data rate allows easy integration of multiple or arrays of detectors and generation of a single real-time stream of UTC epoch'd event data with associated channel ID flags.

This paper describes the upgrades to the HTSI event timer system that enable the high-speed capability. The content will include a data comparison of ILRS stations utilizing the HTSI event timer as well as a discussion of current usage applications and potentials for future use.

High-Speed Enhancement to HTSI Event Timer System

The HTSI Event Timer was designed and built in the 1990s by Charles Steggerda based on his years of experience designing timing devices. Initial laboratory and MOBLAS-7 test results were reported in July 1998 at the 19th International Laser and Radar Conference in Annapolis, MD in a paper titled *Instrumentation Development and Calibration for the Matera Laser Ranging Observatory*. Today's paper follows up after 8 years of use and describes an important new capability that can be utilized by the current and next generation of high rate laser ranging stations. Figure 1 shows the HTSI Event Timer.

Figure 1: *HTSI Event Timer*

HTSI Event Timer Description

The HTSI Event Timer (ET) generates precise epoch time-tags ideal for Satellite Laser Ranging, Lunar Laser Ranging, and other precision timing applications. The ET facilitates measurement of delays between one or more pulses without a range/delay

dependant effect on timing error and supports applications with multiple shots in the air required by high laser fire rates or extended time of flight to targets (i.e. geosynchronous, lunar, or beyond). The basic design and capability hasn't changed since that reported in July 1998 at the 19th International Laser and Radar Conference. The ET couples a precise synchronous counter with from 1 to 4 analog verniers and a computer synchronized to UTC. In the single vernier configuration, the ET provides better than 2 ps of resolution and less than 4 ps of Root-Mean-Square (RMS) jitter. In the four vernier configuration, the ET provides measurement redundancy and increases the effective resolution to <500 fs with an RMS jitter of < 2 ps.

Clock Speed (Internal)	500 MHz, Locks to external 10MHz
Input Channels	12 SMA inputs; NIM type; 50 Ohm termination; negative pulses (unused channels do not require termination)
Resolution	Better than 2ps (1 vernier), 500 femtoseconds (4 vernier)
Dead-Time	100 Nanoseconds
RMS Jitter	<5ps for 1 vernier; <2ps for 4 vernier
FIFO Depth	512
Interface	32 bit DIO, Optional computer allows additional interfaces
Software	UNIX (HP-UX, Linux), MS Windows, etc.
Power	Auto ranging (100-240V; 50-60Hz)

Figure 2: *Summary of Specifications*

Twelve external inputs are provided and events sampled on each channel are tagged with an identification flag in hardware. When coupled with a computer that receives coarse time via time code or GPS, a full event epoch can be generated. Events can be sampled by the hardware at a rate of 10MHz, but are input into a high-speed FIFO buffer that can only store 512 events. Thus the specification of maximum sustainable event sample rate is dependant on the DIO and processing speed of the specific event timer controller.

HTSI Event Timer Past Performance

The initial HTSI event timer development was started in 1995 to support the Matera Laser Ranging Observatory (MLRO). Initial testing of the ET prototype was performed at NASA Goddard Space Flight Center's MOBLAS-7 reference station. Comparison results between the prototype ET and MOBLAS-7 indicated addition of the Event Timer produced an immediate 30-40% improvement in MOBLAS 7 data quality over the existing HP-5370 counter data decreasing LAGEOS range data RMS from 9mm to 5mm.

Later in 1998, the final 4-vernier MLRO and 1 vernier SLR2000 event timers were built. In 2002, a dual vernier model was built for the Global High Accuracy Trajectory Station (GUTS) to be located in Tanegashima, Japan. The MLRO and GUTS event timers supported both stations in achieving best case performance of 2mm ground calibration and 5mm LAGEOS RMS. Both stations utilized the multiple inputs to support fire, dual color PMTs (MLRO), amplified channels for Lunar (MLRO) and Geosynchronous ranging (GUTS), system calibration inputs, on-time pulses, etc. And in 2006, an Event Timer is being built for the US Naval Research Laboratories (NRL)

- **MOBLAS 7** – (Prototype Event Timer; 1998; 3ps RMS)
  - 5 Hz fire, 2 events per frame
  - Use of the HTSI Event Timer produced an immediate 30-40% improvement in MOBLAS 7 data quality over the HP-5370 TIU (Lageos-1 data improved from 9 mm RMS to 5 mm RMS).
- **SLR2000 Prototype** – (Delivered in 1998; 4ps RMS)
  - 2 kHz fire, multiple events per frame, quad PMT
- **MLRO** – (Used in Greenbelt, MD in 1998 and Matera, Italy since 2000; 2ps RMS)
  - 10 Hz fire, 8 events per frame
  - Multiple laser & PMT detection path signals sampled by one event timer.
  - Supported station in achieving 2 mm calibration and 5 mm LAGEOS RMS.
  - Supported station in acquiring two-color and lunar data.
- **GUTS** – (Used in MD in 2002 and Tanegashima, Japan since 2004; 4ps RMS)
  - 10 Hz fire, 4 events per frame
  - Supported station in achieving 2 mm calibration and 5 mm LAGEOS RMS.
  - Supported station in acquiring data from geosynchronous targets.
- **NRL** – Being developed as a stand alone ET for delivery in 2006/2007
- **GUTS Spare** – Being developed for delivery in 2007

Figure 3: *HTSI Event Timer Past Performance*

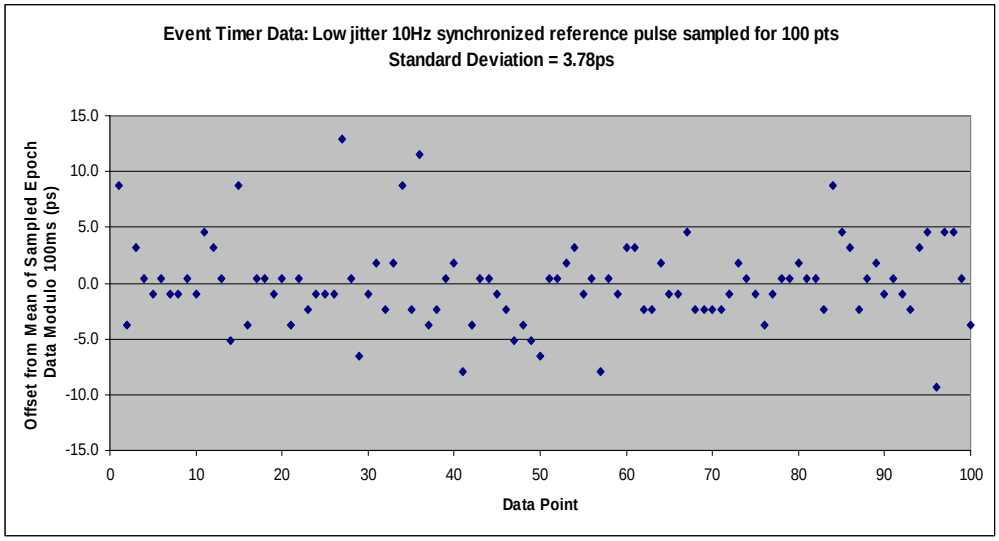

Figure 4: *Event Timer Accuracy*

HTSI Event Timer Data

Figure 4 demonstrates typical Event Timer Accuracy / RMS when configured with a single vernier. To generate this graph, a precise 10Hz electrical reference pulse was sampled 100 times by the event timer. The epoch data was then normalized to the mean repetition frequency. The graph shows raw, unfiltered offset data that demonstrates a 3.78ps RMS jitter. If you look closely, you can see data banding demonstrating that the single vernier bit resolution is <2ps.

Figure 5 demonstrates the potential single shot RMS of stations that utilize the HTSI event timer showing the MLRO and GUTS stations as having the lowest reported LAGEOS single shot RMS in the ILRS network. Note that the event timer, while crucial, is coupled with excellent optics and low-noise optical detection to produce these results.

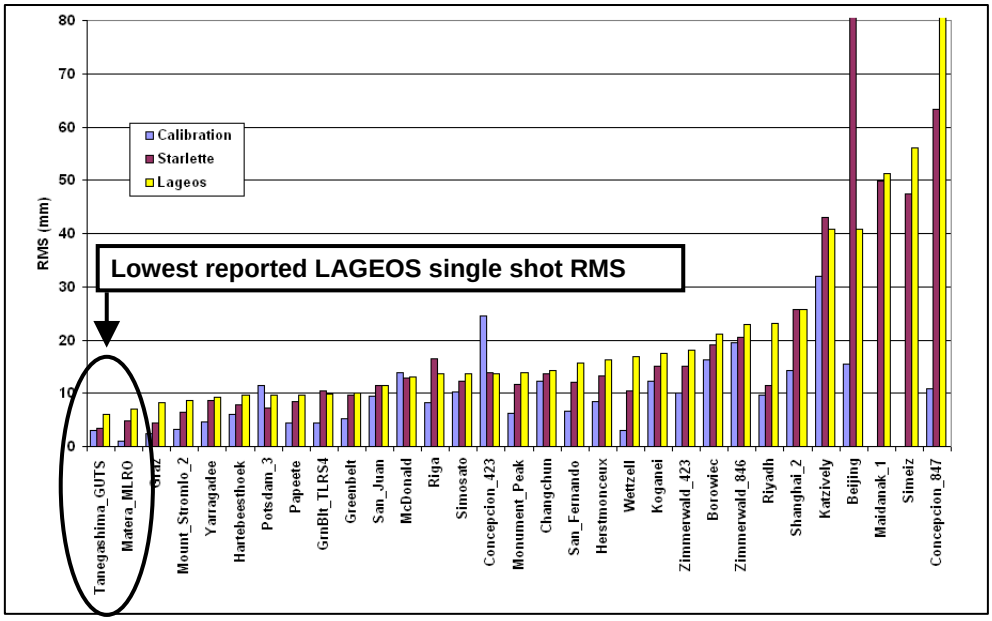

Figure 5: *ILRS Station Single Shot RMS Data for 2Q 2006*

HTSI Event Timer Controller High Speed Enhancement

The HTSI ET has always supported Mega-event per second sample rates, but has been limited by the speed of its control computer in emptying the 512 event deep hardware FIFO. The GUTS and MLRO ET controllers used non-DMA DIO to communicate with the ET at a maximum event rate of approximately 200 events per second (while also performing tracking and controlling other equipment). Counter and verniers were manually addressed by the controller. For SLR2000, HTSI converted the ET to use a high-speed DIO card. In addition, the counter and vernier became auto-addressed allowing for DMA transfer operations. The ultimate data rate was still limited from sharing control computers with other tasks, 10Mbps Ethernet speeds and generation of individual event interrupts.

The advances in computer processing speeds and network bandwidth since 1998 have allowed the design of a high-performance controller to utilize the hardware to its full potential. This high-performance controller enables the HTSI event timer to immediately gain a factor of 10 in sustainable rate (from multi-KHz samples per sec to at least 50ksamples/sec) and promises to allow for further growth in the future as the world transitions to dual core processors and 10GB Ethernet. In addition, the enhanced controller removes the complex issue of DIO interface, driver, and data handling replacing them with a simplistic network accessible design. The enhanced Event Timer controller provides a real-time stream of epoch'd ET data across a dedicated LAN to a station tracking computer. DIO transfer rate is maximized by allowing the ET FIFOs to buffer data. Data is immediately calibrated, combined with UTC coarse time, sent to Ethernet, and received on the tracking computer. A prototype of the enhanced controller has been built in Greenbelt, MD, and is still in the process of software development and testing.

Figure 6 shows the block diagram of the Event Timer Controller that has been built in our integration lab. Notice that all components exist to produce high accuracy time epochs referenced to UTC.

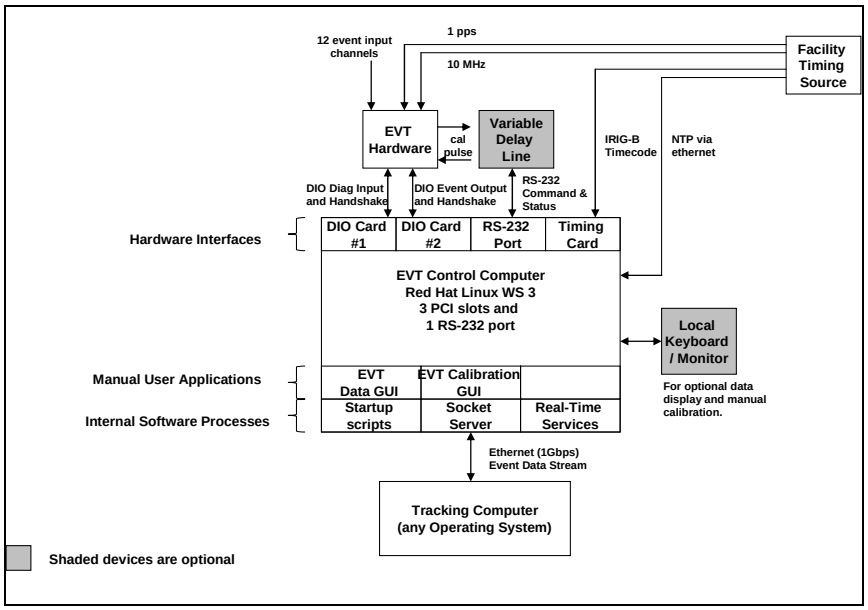

Figure 6: *Enhanced Event Timer Controller: Block Diagram*

Figure 7 shows the internal software architecture and data flows within the Enhanced Event Timer Controller. The Event Timer Software architecture is based on modular C++ UNIX processes inherited from the MLRO and GUTS software heritage. Event Data moves from right to left in this figure. Event Timer and Time Code Generator data is merged to produce a real-time stream of event epoch data. Vernier non-linearity's are then removed via calibration in real-time. The event data is then distributed to client tracking computers via a network socket server.

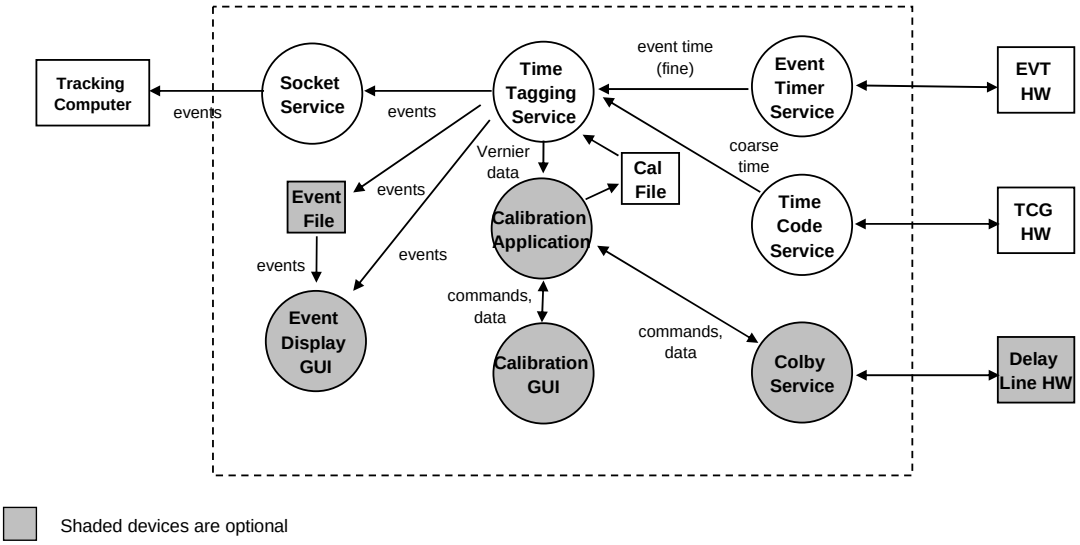

Figure 7: *Enhanced Event Timer Controller Software Architecture*

Optional software modules allow for local calibration of the event timer or independent use of the ET controller by storing event data in a file. Optional modules include a delay line interface, a calibration process and GUI, and an event display GUI.

HTSI Enhanced Event Timer Controller: Initial Results

DIO Performance

Figure 8 shows initial results of high speed testing with the Enhanced Event Timer Controller. Initial DIO laboratory performance tests were able to read reference pulse event times from the ET FIFO buffer at a sustained rate of 5Msamples/sec or **1.25 Million events per second** with a 3 vernier + 1 counter ET. DIO card specifications indicate that the maximum continuous handshaking I/O rate for the DIO-6533 is 17.3 Msamples/sec potentially enabling the reading of. **4.3Million events per second** with a 3 vernier + 1 counter event timer.

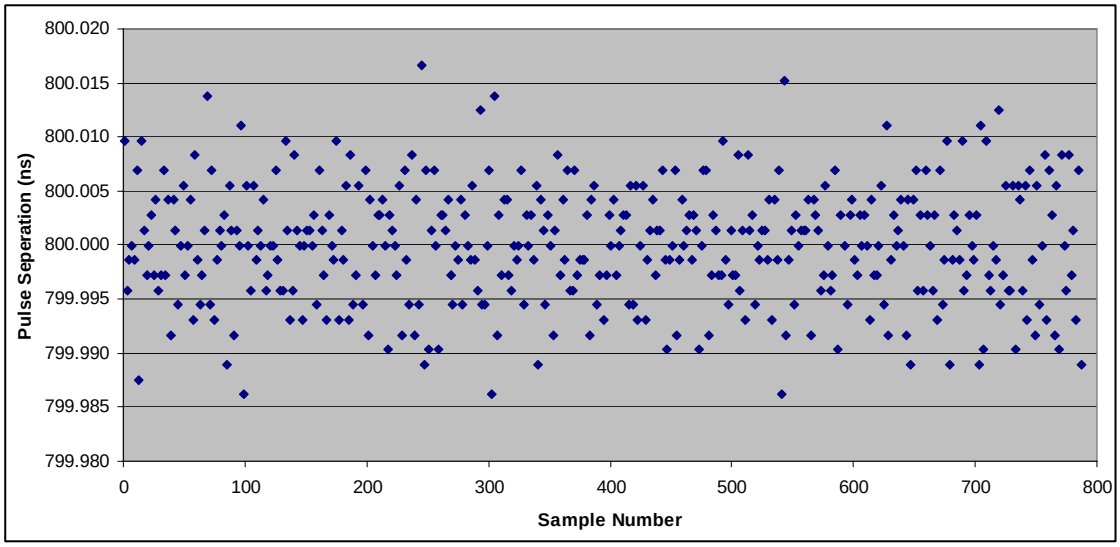

Figure 8: *Initial Enhanced Event Timer Controller High Speed DIO Test Data*

LAN Performance

Preliminary tests demonstrate that it is possible to sustain network transfer rates of **61,035 events per second** on our current 100Mbps testing LAN (no network traffic analysis tool was available to determine actual network bandwidth usage). Further increase in speed is theoretically possible after tuning of packet sizes and enhancing our laboratory with a 1Gbps network switch. These results match initial computations to first order predicting that 50,000 events per second requires a minimum of 25Mbps dedicated network bandwidth on an isolated LAN (assuming 1,024 bit packets holding (8) 112 bit events or 896 bits of user data each and a factor of four compensation for traffic).

HTSI Event Timer: Future Applications

The newly developed HTSI High-Speed Event Timer Controller when combined with the HTSI Event Timer produces a system that can enable many future applications in addition to those currently being supported. Currently the HTSI Event Timer has been used to support:

- 10Hz single and dual laser fire and return with station calibration events (single and multi-wavelength)
- 10Hz geosynchronous and lunar laser ranging (multiple shots in the air)
- 2kHz tracking with 3 high-rate event inputs (6KEvents/sec)

The Enhanced HTSI Event Timer System meets the needs of the SLR data community to acquire data at higher and higher repetition rates with more detectors and enables the design of the next decade of forward reaching experiments. A few of the additional potential applications that can be extrapolated includes:

- 2kHz operations with multiple fire and detection events (i.e. for multiple wavelengths / dual PMTs)
- 2kHz operations with additional station delay diagnostic event inputs
- Use of arrays of detectors at 2kHz (3x3; 3x4; 4x4 would require external event coupling)
- Recording of high rate event epoch data approaching 1 Million events per second
- Laser fire and return pairs several orders of magnitudes faster than 2kHz
- Time transfer experiments (ground and on-orbit)
- Station construction with reduced event timer integration time
- Station construction with reduced real-time tracking controller complexity and cost (ethernet vs. DIO)

References:

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Low-Noise Frequency Synthesis for High Accuracy Picosecond Satellite Laser Ranging Timing Systems

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2. Austrian Academy of Sciences, Observatory Lustbühel

Abstract

The developed Frequency Multiplier from 10 MHz to 200 MHz is fully compatible to the Thales Multiplier and can be directly interfaced to the Thales Event Timing Modules by "plug and play". The new Multiplier designed at Deggendorf University of Applied Sciences shows high sub-harmonic attenuation in the frequency domain of greater than 110 dB.

Whereas, in the time domain the 200 fs rms cycle-to-cycle jitter specification is observed when measuring the output signal with a high-bandwidth sampling oscilloscope. Measurements in the time domain and frequency domain of the new multipliers show better specifications to existing frequency synthesizers.

The 10 MHz to 80 MHz Frequency Multiplier is in continuous operation at Mount Stromlo SLR Station and in various Keystone SLR Stations in Japan. Modules are available through our partner company MPF Optics Ltd.

Introduction

Tests carried out at SLR station Lustbühel, Graz:
Graz E.T. / Dassault Modules:
Comparison between Dassault Clock and Deggendorf-Clock

- DeggendorfClock is mechanically / electrical connections identical to Dassault Clock;
- Measurements in Graz were made using both clock modules alternatively;
- Measurement description:
    - Standard Laser Firing pulse (TTL), Power Splitter 50 Ohm;
    - 1 Pulse direct into E.T. Start;
    - Splitted pulse delayed with cable, into E.T.Stop;
    - Standard Calibration Program used, Single Time Intervals stored;
    - Results checked with Program DRAW, 2.2 Sigma Iteration;
- For ease of tests: Clock module 200 MHz outputs (both clocks) connected via standard RG58 Cables / SMA connectors into Start / Stop Modules (instead of Dassault Semi-Rigid Cables). All Tests performed in this configuration.
- At each change of Setup: E.T. switched off; new sync / new offsets after each switch on.

Results (in ps) / No Sigma iteration

Cal_1: 9215.94 ± 3.87 [ps]	Dassault Clock	Semi-Rigid Cables (Graz Original Setup)
Cal_2: 9216.04 ± 3.34 [ps]	Dassault Clock	RG 58 cable
Cal_3: 9217.14 ± 3.58 [ps]	Deggendorf clock	RG 58 cable
Cal_4: 9214.83 ± 3.34 [ps]	Dassault Clock	RG 58 cable
Cal_5: 9216.45 ± 3.32 [ps]	Deggendorf clock	RG 58 cable

Results (in ps) / 2.2 Sigma iteration:

Cal_1: 9215.94 ± 2.84 [ps]	Dassault Clock	Semi-Rigid Cables (Graz Original Setup)
Cal_2: 9216.12 ± 2.79 [ps]	Dassault Clock	RG 58 cable
Cal_3: 9217.00 ± 2.82 [ps]	Deggendorf clock	RG 58 cable
Cal_4: 9214.73 ± 3.07 [ps]	Dassault Clock	RG 58 cable
Cal_5: 9216.45 ± 2.57 [ps]	Deggendorf clock	RG 58 cable

Remarks

- Variation in absolute values (1-2 ps): Due to new offsets between start/stop modules after switch ON.
- Several other calibration runs were made, with different cable length etc.; all giving similar results.
- The Deggendorf clock module seems to have at least the same specs than the Dassault; no difference visible.

Editor's Note

The technical data specification for the frequency multiplier unit can be found on the accompanying CD.