

Graz Event Timing System: E.T.

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SLR GRAZ

Using the commercially available Event Timer Modules from Dassault, a new Event Timing System (E.T.) has been designed and built for the Graz SLR station. Using 2 modules (plus the necessary clock module) for a simple start/stop system – with optional upgrades for a total of 4 channels to include later MultiColor ranging -, it is in operation since 08/2000.

The Dassault modules deliver < 2 ps RMS, and < 2.5 ps linearity error; we have designed and built in addition a special input board, which allows PC-controlled selection of up to 3 different inputs to each module: Signal / 1-pps / 1-kHz pulses. The 1 pps pulses can be applied to all modules, allowing real epoch timing; the 1-kHz pulses are used to determine and eliminate any offsets between the modules (ZEROing of inputs). All modules are connected to / controlled by our standard Real-Time Ranging PC via a 96-bit DIO interface; this and the software developed allows measurement rates of up to 2.5 kHz for all modules.

Using this E.T. within the Graz SLR system, we get about 3 mm for routine calibrations and for satellites like ERS-2 or Champ. Using higher return signal strengths of 2000 photons (during test calibrations only), the total system single shot RMS is now exactly 1.0 mm.

1.0 The Hardware

1.1 Requirements

Our goal was to build an universal Event Timer (named **E.T.**) and Time Interval Counter, which is completely controlled via some standard PC interface, and keeps all the specified performance of the single modules. This means that all added circuitry:

- Should not degrade the RMS / linearity / temperature specification of the single modules
- < 2 ps RMS; < 2.5 ps linearity error;
- 0 - 40 °C operating temperature;
- maximum repetition rate 2.5 kHz

- Should allow for up to 4 independent channels or modules;
- 2 required as minimum for Start/Stop Time Intervals;
- 2 more for MultiColor Ranging etc;

- Should allow for independent Epoch Timing OR Time Interval Measurements;
- BOTH with ALL resolution and accuracy as delivered from the modules;
- Automatic Epoch Referencing via 1-pps-pulses from external GPS device;

- Should allow for Automatic Internal Offset Determination/Elimination between Modules;
- The PC interface and software should not reduce the maximum repetition rate (2.5 kHz);
- The PC interface and software should not degrade the high resolution of the modules;
- The E.T. should be capable of serving as High Performance Timer for routine operation at SLR Graz without any additional workload, service or calibration requirement etc.



1.2 Implementation

A block diagram of the E.T. hardware is in fig. 1: Our standard Laser Ranging PC houses a 96 Bit Digital I/O Card (PC-DIO-96 from National Instruments); all 96 bits are connected to the Graz Input PCB; up to 25 Power Supplies are delivering separate and independent voltages for the timer modules, the clock module and the Input PCB.

1.2.1 The PC-DIO-96 Card

Each of the up to 4 modules uses 24 bits of this card:

- 16 bits are used for data transfers from module to the PC
- 3 bits are used for handshaking between PC and modules;
- 1 bit is used to switch the 1-pps from the HP GPS into the modules input (Event Time Sync);
- 1 bit is used to switch the 1 kHz from the Graz Input PCB into the modules input (Module Offset Determination / Elimination);
- 1 bit is used to detect the 1-pps pulse presence (for system status, tests etc.);
- 2 bits are spare for each module; at module #1, 1 of these spare bits is used to detect the 10-MHz pulse presence (for system status checks etc.)

The card is connected to the Graz Input PCB via standard 100 line cable and connectors, allowing to supply also 5 V and GND to the PC-side of the Graz Input PCB Interface.

1.2.2 The Graz Input PCB

As stated above, our main goal was not to degrade the Dassault modules specifications; this means that we had to be extremely careful with the design for the Input PCB, as all timing pulses are routed via this PCB into the Dassault modules. This involves strictly separated GND and Power Supplies for the different parts (PC-Side of Control Logic, Module Side of Control Logic, ECL part of routing logic etc.), using Opto-Couplers where applicable (for switching control pulses only).

The input PCB has to handle/switch/enable 3 different pulses (fig. 2):

- Input pulses: ECL; standard start / stop pulses from the C-SPAD etc.;
- 1-pps pulses as delivered from HP GPS device;
- 1 kHz pulses produced on the PCB

For all 3 pulses we avoid any switching elements, to eliminate all effects of non-reproducible resistances/voltages etc.; instead we use the different inputs of fast comparators (AD966879); while its outputs always deliver uniform standard ECL pulses into the modules, both inputs are used for switching/triggering 1 of the 3 pulses (whichever is enabled via PC control) via capacitive coupling.

The 16 data bits and the 3 handshake bits are connected direct to the modules, bypassing the Graz Input PCB.

1.2.3 Power Supplies

Using separate power supplies for each module, PC interface and Graz Input PCB, ends up in a significant number of supplies (up to 25 with 4 timer modules); to minimise heat generation /size / power losses etc. each supply was optimised / minimised for its specific purpose; a separate fan is removing the heat from these power supplies (a second fan is doing this for the modules section, see fig. 3)

2.0 Software

The E.T. is completely controlled via the 96-bit DIO interface; although this interface offers also high level programming, we decided to use simple register programming via low level FORTRAN subroutines; although this requires a bit more time for writing, it offers maximum speed during execution. A set of about 30 low-level FORTRAN subroutines (doing register setting, bit manipulations etc.) now allows easy access to the full E.T. functionality:

- Handling all initialising / setting /resetting of the modules;
- Monitoring of module status, results availability etc.;
- Reading available result bit streams from each module (64 bits per measurement);
- Calculating Epoch Times, Time Intervals etc. with 64 bits resolution;
- Routing 1-kHz pulses to all modules for Automatic module offset determination / elimination;
- Routing 1-pps to all modules for Epoch Time referencing etc.;

Special routines have been developed to handle the 64 bit long results of each module; this was solved by writing dedicated arithmetic routines working on a bit-by-bit basis; this allows to use the full resolution for epoch time differences (i.e. time intervals) or to select any required solution for Epoch Timing; it would be easy scalable up to higher bit numbers, if such timers should appear

3.0 Results

After completing all functional tests, we started to check the performance; one of the first tests was a measurement of the warm-up drift (fig. 4); the E.T. was switched off completely during night; the instrument was switched on, and measurements started immediately; 500 measurements of a cable delay were averaged and stored for each data point; during the first 10 minutes, the results drifted about 2.5 ps (fig. 4); during the next 1.5 hours, the results remained within ± 0.8 ps.

Extending the measurement period to about 16 hours (fig. 5), the results still remained within 1 ps maximum deviation, demonstrating the excellent stability of modules and our circuits!

The E.T. was implemented into the Graz SLR system during August 2000, and used for routine ranging since day 202/2000; offsets between event timing modules 1 and 2 are measured and stored automatically during each routine calibration; these offsets are in the range of a few ms – and may differ in the ms-range after each power-on reset. Measuring, storing and using these offsets allows complete elimination of these offsets, effectively “ZEROing” all E.T. inputs. Fig. 6 shows the stability of these offsets over the period from day 200/2000 (when we started routine operation with E.T.) until day 360/2000 (a power failure on day 005/2001 caused completely new offset values); all measurements show excellent picosecond stability over almost half a year!

The main limitation for the SLR Graz accuracy at the moment is – for the single photon level – the C-SPAD; reducing this contribution by increasing the return signal strength to at least 1000 photons, the Graz SLR system delivers an RMS of 1 mm to the calibration target (fig. 7).



Graz Event Timing System - E.T.

General Setup

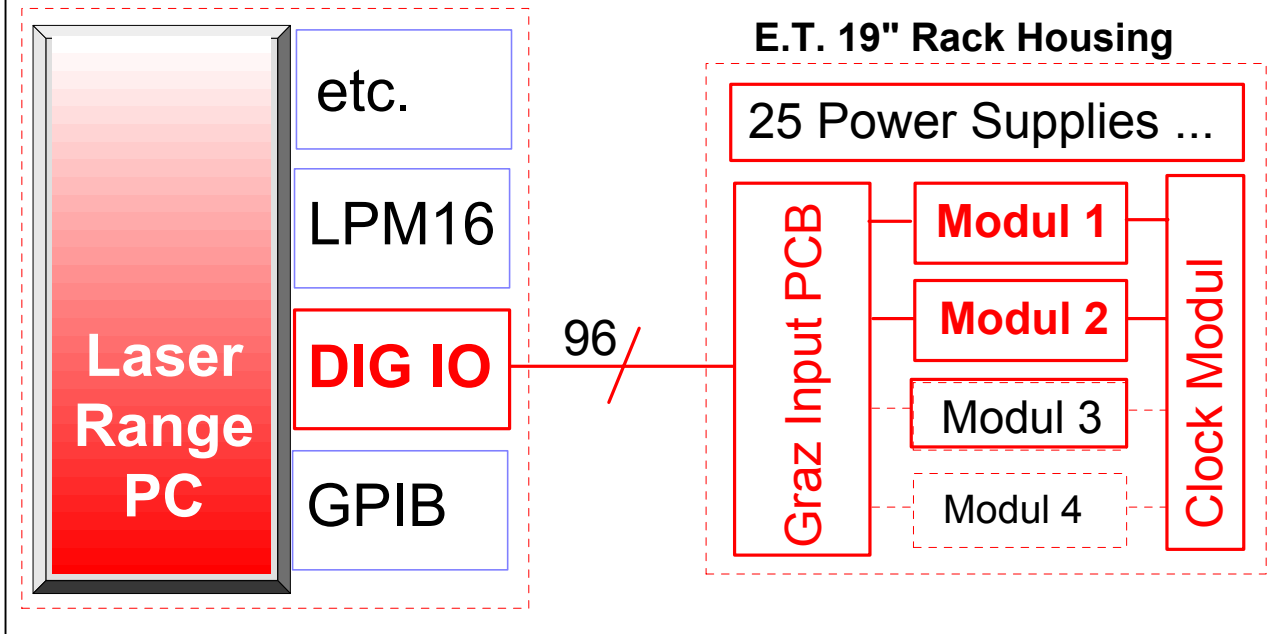


Fig. 1: Block Diagram of Graz E.T.

Input Board Concept - E.T.

Each Modul accepts 3 Sources: Signal / 1 pps / 1 kHz; PC selected

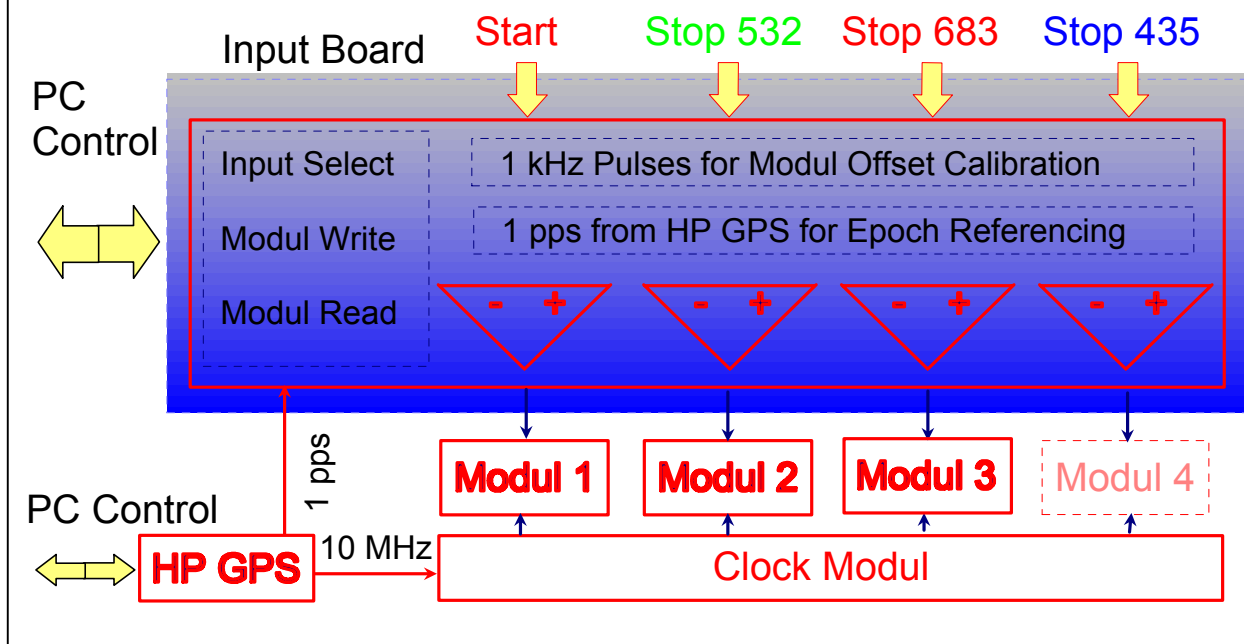


Fig. 2: Graz Input PCB Concept



Fig. 3: 19" Rack Module, with 2 Event Timer Modules, Clock Module, Input Board, Power Supply

GRAZ E.T.: WARM-UP DRIFT

Switched Off During Night
Immediate Start after Switch-ON

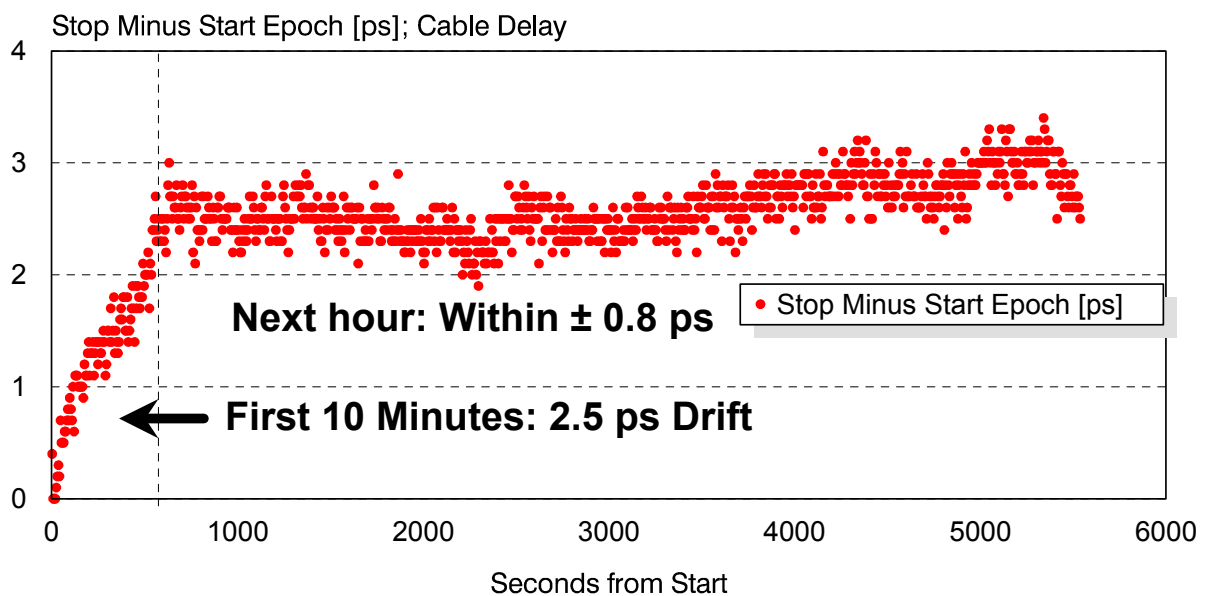


Fig. 4: Warm-Up Drift; after 10 minutes, stability is better than ± 0.8 ps

GRAZ E.T.: Half-Day Drift

Start: AFTER 10 Minutes Warm-Up

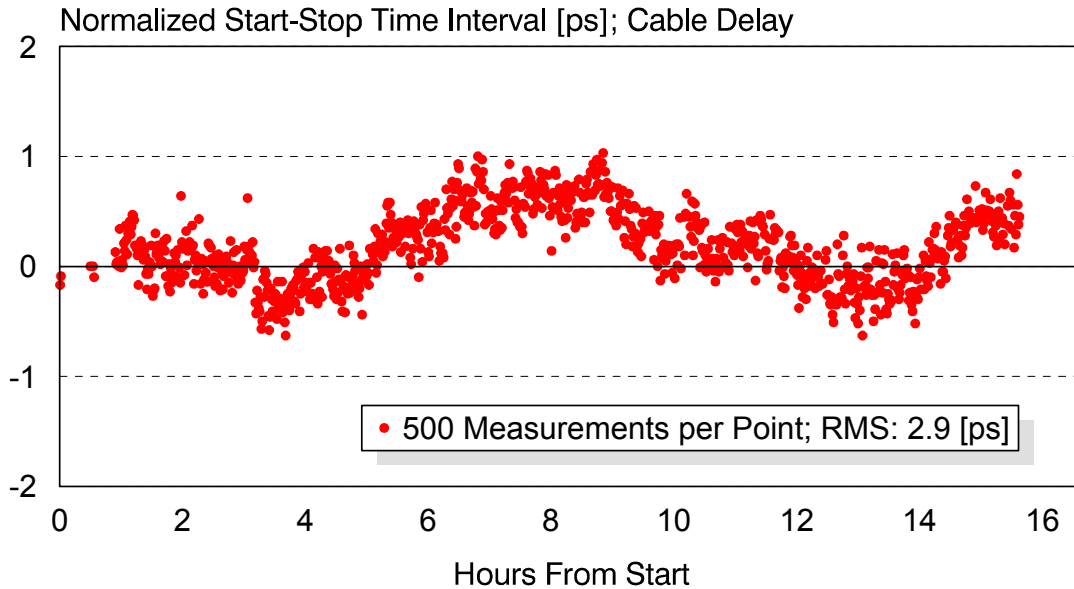


Fig.5: Stability over 15 hours: Better than ± 1 ps

E.T.: Offsets between 2 Channels

Stability during 160 Days Ranging / 6844 Cals

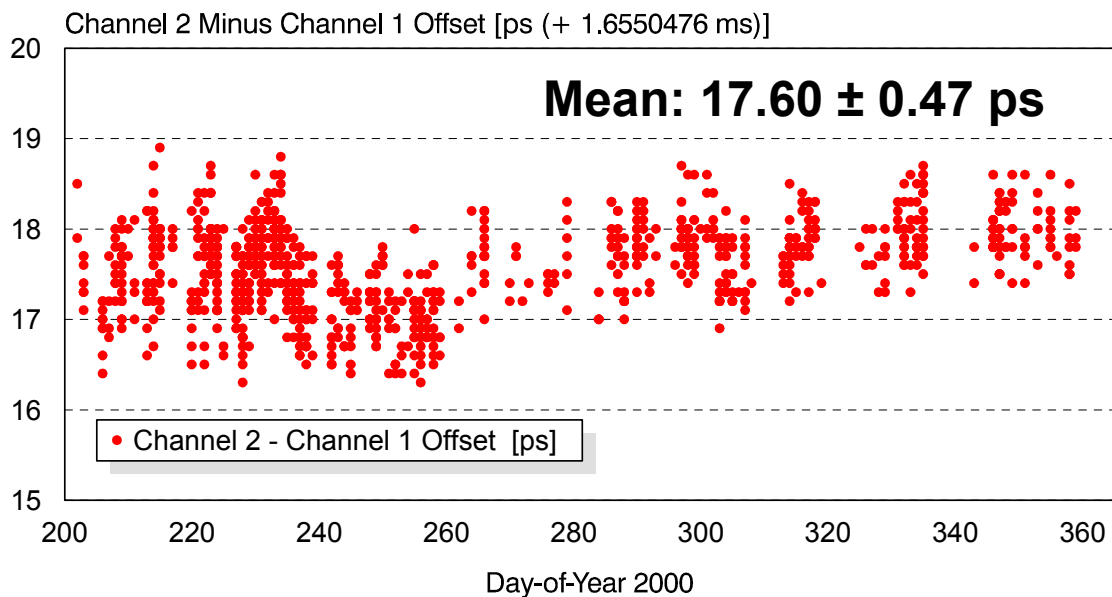


Fig. 6: Offsets between 2 Event Timer Channels, measured at routine calibrations of year 2000

Graz Event Timer - E.T.

System CAL vs. Signal Strength

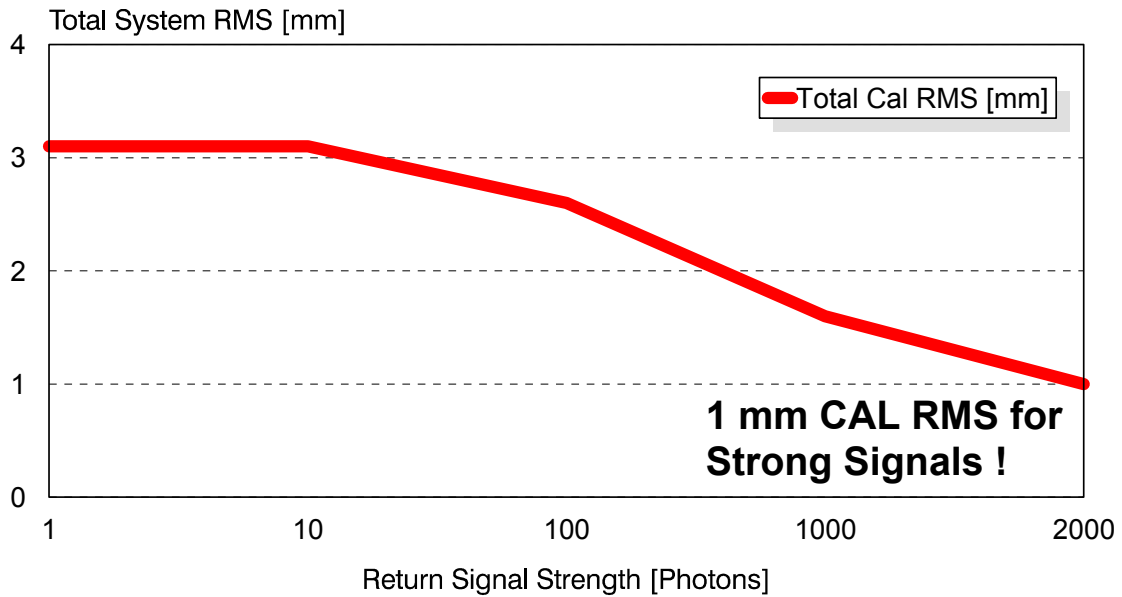


Fig. 7: Total System RMS: 1 mm for Strong Return Signals



We like **E.T.**